HIGH FREQUENCY WAVEFORM GENERATOR

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ABSTRAD

This Project comes from the necessity of getting a wave generator with a bandwidth over 10 Mhz and an harmonic distortion under 1%, all of this with a low cost price.

This document describes a design of a wave generator with a bandwidth over 10MHz , which produce: sine, triangle, sawtooth, or square (pulse) waveforms with an harmonic distortion under 1%, duty-cycle adjustment, frequency modulation, TTL output and offset voltage. It is also presented the design of a frequency counter.

INDEX

INTRODUCTION.

1.1 Goals.

Making a waveform generator of low cost with the following characteristics:

- Bandwidth over 10MHz.
- Waveform generator of sine, square and sawtooth.
- Typical harmonic distortion under 1%.
- Duty cycle adjust.
- Offset voltage.
- Frequency modulation.
- TTL output.

Also the generator has a LCD screen in which it shows the frequency and the peak voltage from the waveform

1.2 The MAX038

1.2.1 Characteristics

The MAX038 is a high-frequency function generator that produces low-distortion sine, triangle, sawtooth, or square (pulse) waveforms at frequencies from less than 1Hz to 20MHz or more, using a minimum of external components..

1.2.2 Working

The MAX038 (see PDF) has a basic type of relaxation oscillator, that operates by alternately charging and discharging a capacitor, with constant currents. Basically it is a dual slope integrator that simultaneously produces a triangle wave and a square wave (TTL). The frequency is determined by the external oscillator capacitor and the flowing current into IIN. This internal triangle wave is applied to an internal comparator, in order to make a square wave. The sine wave is got applying the triangular wave to a shaper waveform sine circuit that correct it automatically and it produces a sine wave with a distortion under 1% and a constant amplitude. The triangle, square, and sine waves are input to a multiplexer that select the type of wave which is applied to the low impedance separating amplifier.

Problem description.

The waveform generator will have two main parts: the waveform circuit and the supply. Also the waveform generator will have a buffer connected to the output signal, in order to connect a frequency counter

1.3 The waveform generator.

As we can see the chip MAX038 is the generator itself ,although it needs an external easy circuit to implement its characteristics, and also the ones described in the objectives.

Taking into account this and its characteristics, it has the following parts within the waveform generator.

- Frequency adjust.
- Frequency range selection.
- Kind of waveform selection.
- Duty cycle adjust.
- Offset voltage.
- Frequency modulation generator.
- Analogical output with level amplitude control.
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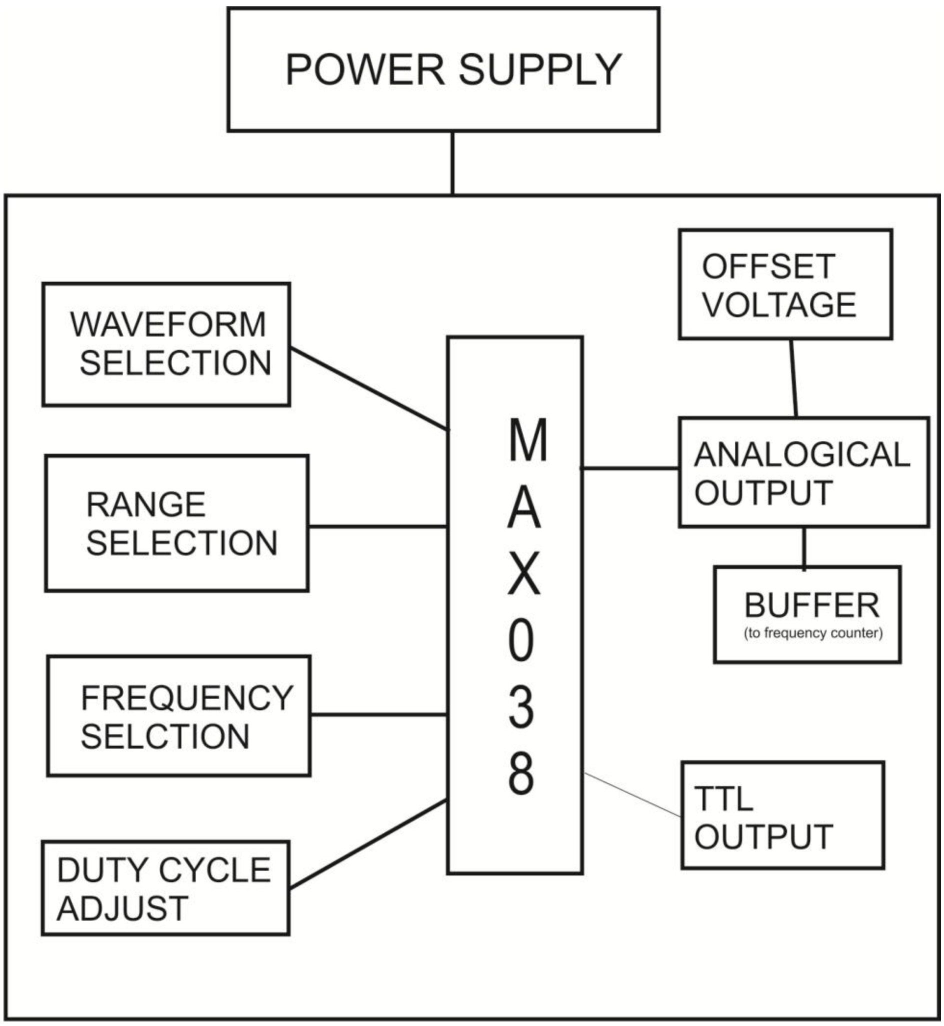
Another important fact will be the distribution of the components and the nets , because in order to work with high frequency and to keep low levels of distortion, it will be necessary taking into account some electromagnetic compatibility rules.

1.4 Power Supply.

The supply will be the one which transform 220V voltage into the different voltages that the generator need for work in a proper way.

1.5 System diagram.



TAKEN SOLUTION.

1.6 Waveform generator.

As we can see, the chip MAX038 makes all the work , it just need an easy circuit in order to implement its characteristics.

1.6.1 Frequency adjust.

The output frequency is determined by three factors. The first is the oscillator capacitor value from the CF (pin 5), that set the internal work frequency. The second one is the flowing current into IIN (pin 10). The third one is the voltage on FADJ (pin 8). The last one is used only for fine adjust of the frequency or for frequency modulation, because it have only about the 70% of the range respect IIN.

The equation that determine the frequency according to these three factors is:

Fx = Fo x (1 – [0.2915 x VFADJ])

Fx = output frequency

Fo = frequency when VFDJ = 0

Fo (MHz) = IIN(uA) ÷ CF (pF)

ADJUST IN THE PIN IIN

This pin works like a virtual ground, so it is just necessary to supply a voltage through a resistor (R8). In order to provide a stable reference voltage, it is used an operational amplifier like a follower voltage (U1B), which takes the voltage from the pin REF (2.5V). The resistors R6 and R7 limit the value of voltage supply to R8 , in order to be inside of its lineal range of work.

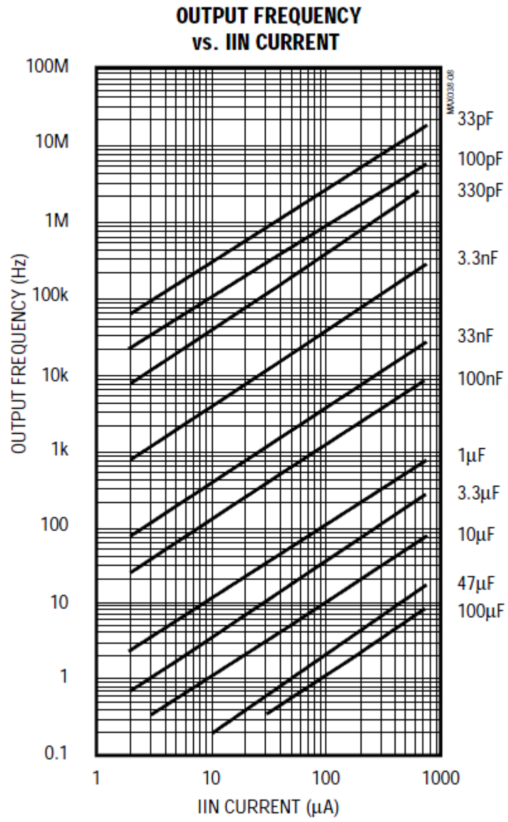


Figure 3.1.1.- Output Frequency VS. IIN Current

ADJUST ON PIN FADJ

The voltage supply to this pin, comes from an operational amplifier working like a follower voltage. R3 and R4 are used to make a voltage divisor and set it between its linearity range. R5 and C5 work like a low-pass filter.

This part of the circuit is susceptible to the interference appearances, because a little voltage variation will produce a frequency change. So , a supply that generate curly voltage will produce distortion through this part of the circuit.

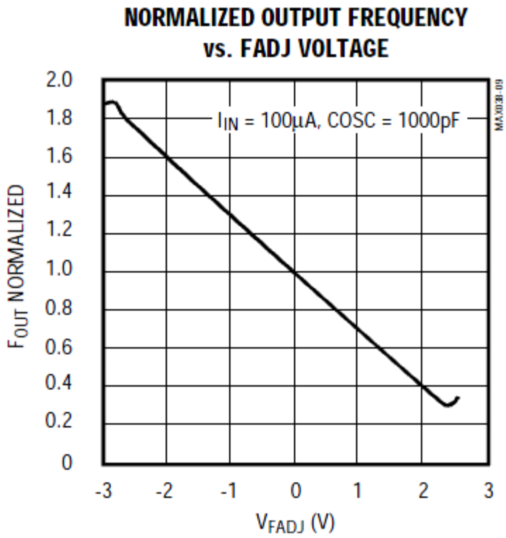


Figure 3.1.2.- Normalized Output Frequency vs. FADJ Voltage

1.6.2 Frequency range selection.

The capacitors C1, C2, C3 and C4 let to provide a bandwidth from 2Hz to 20MHz, with four frequency ranges, which will be overlapped.

In this part f the circuit, it is fundamental to avoid the parasitic capacity in order to get the estimated bandwidth limit, because, as it is explained in the chapter 1.2.2, the generator works charging and discharging a capacitor, so fewer capacity higher the frequency. For that, the capacitors are connected to the pin COSC from the chip, and the selection of these will be made through the connection of those to the ground ,using transistor like an interrupter.

The voltage in the pin COSC , changes from 0 to -1V. the polarised capacitors are not recommended to this part, but if they are used , the positive pin will be connected to ground and the negative one to the pin COSC. The propylene capacitors will be the best option, but also ceramics capacitors can be used, because they are cheaper and they are completely satisfactory to this purpose.

1.6.3 Type waveform selection.

The sine Squire triangular functions are selected by the switch SW2.A0 and A1 are digital selected inputs of the MAX038 that select by an internal multiplexer, the function which has to be applied to the output.

Switching occurs within 0.3µs, but there may be a small transient in the output waveform that lasts 0.5µs.

A0	A1	WAVEFORM
X	1	Sine wave
0	0	Square wave
1	0	Triangle wave

Figure 3.1.3.- Type waveform selection

1.6.4 Duty cycle adjst.

The voltage in the DADJ pin controls the work cycle of the output waveform (defined as the time percentage in which the output waveform is positive). Usually VDADJ is equal to 0, and the duty cycle is the 50%. The variation of this voltage between ±2,3V will produce a variation of the duty cycle that change from 15% to 80%.

The used circuit for this purpose comes from the PDF (of the MAX038), although it also could have been used a circuit like the one of the fine frequency adjustment.

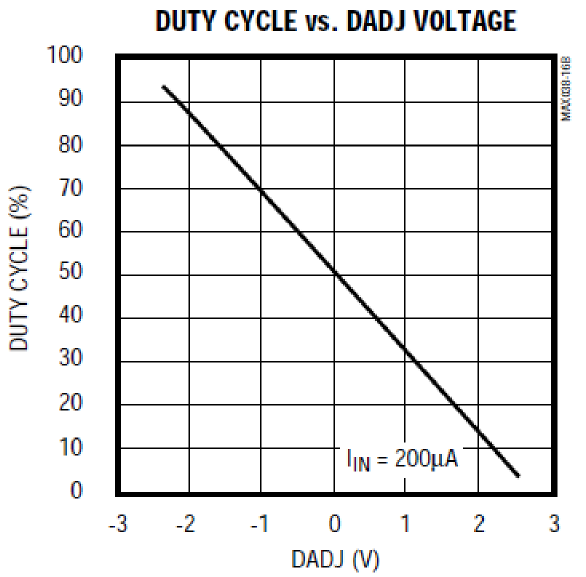


Figure 3.1.4.- Duty cycle VS DADJ Voltage

1.6.5 Frequency modulation

For this purpose, it could be used the inputs IIN, FADJ and DADJ. In this case, it is just used the FADJ input. The only thing that it is necessary to produce modulated frequency is to introduce a modulating signal for this input, with a maximum frequency of 2MHz.

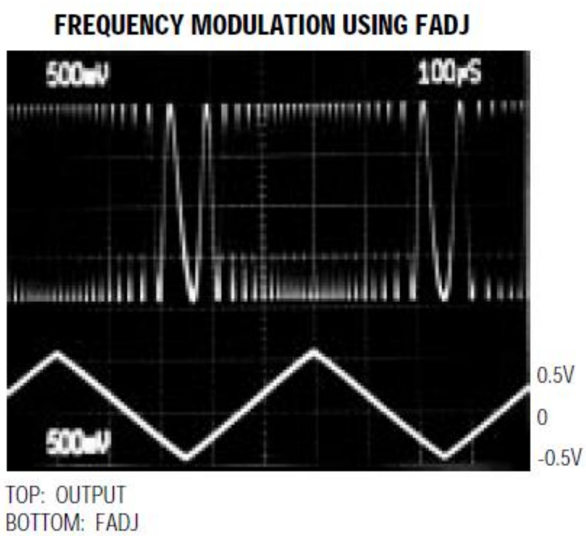


Figure 3.1.5.- Frequency modulation using FADJ

1.6.6 TTL output

The digital output TTL is got directly from the pin SYNC. This signal change its state from high to low , each time that the analogical output goes through 0V with a positive direction.

The output SYNC has its own supply pin, which has to be separated from the general supply. This is very important in the moment to design the PCB, if it is not in this way, in the analogical output will appear a small peak, each time the output of digital synchronism changes its state.

1.6.7 OFFSET voltage.

The Offset voltage is a positive or negative D.C. that is applied to the signal.

For this purpose, it is used an operational amplifier like follower, in order to give a stable voltage reference.

1.6.8 Analogical output.

The analogical output of MAX038 produce a Peak voltage of 2V for every kind of waveform. This output after the operational amplifier is of low impedance, so it is necessary a 50OHM resistor to adapt the signal to the established standards. We use an operational amplifier in order to have more output voltage. For this it is used the operacional OPA 2690 (http://www.ti.com/lit/ds/symlink/opa2690.pdf**)** Although we can use another operational with a bandwidth over 150MHz,because the squared signals consisted on its fundamental frequency plus its odd harmonics, so bigger the bandwidth bigger the quality of the squared wave, which can go through it.

The output of this circuit is connected to an operational working like adder, in which the analogical signal is connected to the inverting input and the OFFSET signal to the positive input, in this way, avoiding interferences between both circuits. This adder circuit will have in its output a 47 ohms resistors, in order to adapt the output to the standards. It must be taking into account that these resistors is not always necessary, because the most of BNC connectors have this resistor implemented.

1.6.9 PCB design.

For the PCB design, we have to think about some rules of electromagnetic compatibility ,either in the components emplacement or the nets route.

Components emplacement

It is the first thing we have to make when we start with the PCB design. A good emplacement of the components will make easier the nets route.

Decoupling capacitors: Decoupling capacitor should usually be placed as close as possible to the device requiring the decoupled signal, in this case close to supply's pins of the chips.

Filter capacitor: Filter capacitors also should be placed as close as possible to the noise resource, for example to the commutated output supply.

Microprocessors: They must be emplaced far away from the noise resources or high currents.

Crystals: Crystals should be placed as close as possible to the clock inputs pins of the microprocessor.

Power drivers: they must be distant from sensitive components such as microprocessors, crystals, communication components, etc… It is also convenient that they are as close as possible to the output pins from the connector to which it is connected.

1.6.10 Net route

It is necessary to take into account the following rules:

It must be routed firstly the main signal nets and the sensitive nets to the EMI (electromagnetic interference). It is also convenient to shield them with ground nets.

The nets that have high fluctuating currents must be routed as far as possible to the sensitive nets.

The supply nets must be routed with star shape, that is, we must distribute the supplies to different circuit's areas and all of them must begin in the main filter capacitor.

The supply nets have to go perpendicular to the signal ones, in order to avoid interferences with these.

The ground plans must be joined for one point, in order to avoid closed loops which can generate noise.

1.7 Power supply

The power supply changes from 240 AC voltage to the different DC voltages, that the generator needs to work properly.

The power supply is a typical regulated symmetric supply. The diodes D6 and D8 work protecting the regulators against the discharge from the capacitors. D11 and D12 to protect the supply against the external circuit to it.

It also has two fuses, in the output of the bridge diode circuit, in order to protect the waveform generator against short-circuits.

The capacity of the capacitors must not be lower than the capacities described in the schematic, because this is a simple power supply and need big values of capacity for the capacitors, in order to have a little ripple voltage. We have to be in account that the most of the distortion that it is produced in the waveform came from the supply.

APPENDIX

MAX038

19-0266; Rev 3a; 4/01

EVALUATION KIT AVAILABLE

MAXIM

High-Frequency Waveform Generator

MAX038

General Description

The MAX038 is a high-frequency, precision function generator producing accurate, high-frequency triangle, sawtooth, sine, square, and pulse waveforms with a minimum of external components. The output frequency can be controlled over a frequency range of 0.1Hz to 20MHz by an internal 2.5V bandgap voltage reference and an external resistor and capacitor. The duty cycle can be varied over a wide range by applying a ±2.3V control signal, facilitating pulse-width modulation and the generation of sawtooth waveforms. Frequency modulation and frequency sweeping are achieved in the same way. The duty cycle and frequency controls are independent.

Sine, square, or triangle waveforms can be selected at the output by setting the appropriate code at two TTL-compatible select pins. The output signal for all waveforms is a $2V_{P-P}$ signal that is symmetrical around ground. The low-impedance output can drive up to ±20mA.

The TTL-compatible SYNC output from the internal oscillator maintains a 50% duty cycle—regardless of the duty cycle of the other waveforms—to synchronize other devices in the system. The internal oscillator can be synchronized to an external TTL clock connected to PDI.

Features

- **0.1Hz to 20MHz Operating Frequency Range**
- **Triangle, Sawtooth, Sine, Square, and Pulse Waveforms**
- **Independent Frequency and Duty-Cycle Adjustments**
- **350 to 1 Frequency Sweep Range**
- **15% to 85% Variable Duty Cycle**
- **Low-Impedance Output Buffer: 0.1Ω**
- **Low-Distortion Sine Wave: 0.75%**
- **Low 200ppm/°C Temperature Drift**

Ordering Information

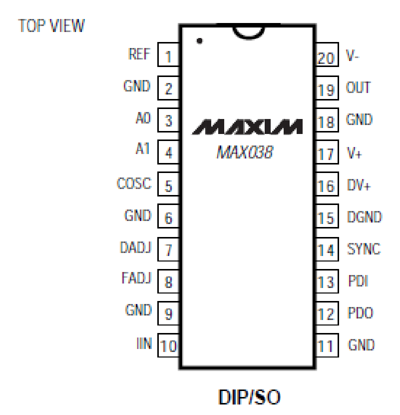
PART	TEMP. RANGE	PIN-PACKAGE
MAX038CPP	0°C to +70°C	20 Plastic DIP
MAX038CWP	0°C to +70°C	20 SO
MAX038C/D*	0°C to +70°C	Dice*
MAX038EPP*	-40°C to +85°C	20 Plastic DIP
MAX038EWP*	-40°C to +85°C	20 SO

Contact factory.

Applications

Precision Function Generators
Voltage-Controlled Oscillators
Frequency Modulators
Pulse-Width Modulators
Phase-Locked Loops
Frequency Synthesizer
FSK Generator—Sine and Square Waves

Pin Configuration



High-Frequency Waveform Generator

ABSOLUTE MAXIMUM RATINGS

V+ to GND ....-0.3V to +6V
DV+ to DGND ....-0.3V to +6V
V- to GND ....+0.3V to -6V
Pin Voltages
IIN, FADJ, DADJ, PDO ....(V- - 0.3V) to (V+ + 0.3V)
COSC ....+0.3V to V-
A0, A1, PDI, SYNC, REF ....-0.3V to V+
GND to DGND ....±0.3V
Maximum Current into Any Pin ....±50mA
OUT, REF Short-Circuit Duration to GND, V+, V- 30sec

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SO (derate 10.00mW/°C above +70°C) 800mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX038C_ _ ....0°C to +70°C
MAX038E_ _ ....-40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, GND = DGND = 0V, V+ = DV+ = 5V, V- = -5V, V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO} = 0V, C_F = 100pF, R_{IN} = 25kΩ, R_L = 1kΩ, C_L = 20pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY CHARACTERISTICS						
Maximum Operating Frequency	F_O	15pCF ≤ 15pF, I_{IN} = 500µA	20.0	40.0		MHz
Frequency Programming Current	I_{IN}	V_{FADJ} = 0V	2.50		750	µA
		V_{FADJ} = -3V	1.25		375	
IIN Offset Voltage	V_{IN}			±1.0	±2.0	mV
Frequency Temperature Coefficient	$\Delta F_O/°C$	V_{FADJ} = 0V		600		ppm/°C
	$F_O/°C$	V_{FADJ} = -3V		200		
Frequency Power-Supply Rejection	$\frac{(\Delta F_O/F_O)}{\Delta V+}$	V- = -5V, V+ = 4.75V to 5.25V		±0.4	±2.00	%/V
	$\frac{(\Delta F_O/F_O)}{\Delta V-}$	V+ = 5V, V- = -4.75V to -5.25V		±0.2	±1.00	
OUTPUT AMPLIFIER (applies to all waveforms)						
Output Peak-to-Peak Symmetry	V_{OUT}			±4		mV
Output Resistance	R_{OUT}			0.1	0.2	Ω
Output Short-Circuit Current	I_{OUT}	Short circuit to GND		40		mA
SQUARE-WAVE OUTPUT (R_L = 100Ω)						
Amplitude	V_{OUT}		1.9	2.0	2.1	V_{P-P}
Rise Time	t_R	10% to 90%		12		ns
Fall Time	t_F	90% to 10%		12		ns
Duty Cycle	dc	V_{DADJ} = 0V, dc = t_{ON}/t x 100%	47	50	53	%
TRIANGLE-WAVE OUTPUT (R_L = 100Ω)						
Amplitude	V_{OUT}		1.9	2.0	2.1	V_{P-P}
Nonlinearity		F_O = 100kHz, 5% to 95%		0.5		%
Duty Cycle	dc	V_{DADJ} = 0V (Note 1)	47	50	53	%
SINE-WAVE OUTPUT (R_L = 100Ω)						
Amplitude	V_{OUT}		1.9	2.0	2.1	V_{P-P}
Total Harmonic Distortion	THD	Duty cycle adjusted to 50%		0.75		%
		Duty cycle unadjusted		1.50		

ELECTRICAL CHARACTERISTICS (continued)

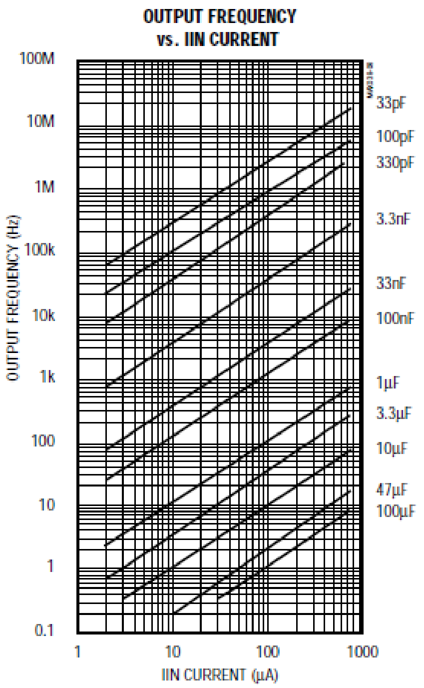
(Circuit of Figure 1, GND = DGND = 0V, V+ = DV+ = 5V, V- = -5V, V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO} = 0V, C_F = 100pF, R_{IN} = 25kΩ, R_L = 1kΩ, C_L = 20pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

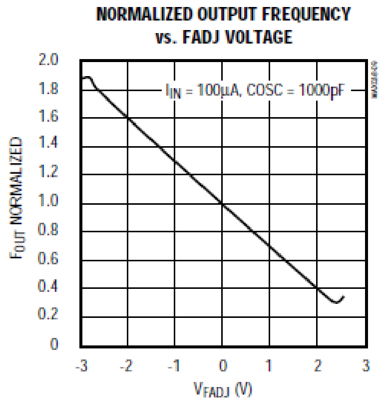
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC OUTPUT						
Output Low Voltage	V_{OL}	I_{SINK} = 3.2mA		0.3	0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 400μA	2.8	3.5		V
Rise Time	t_R	10% to 90%, R_L = 3kΩ, C_L = 15pF		10		ns
Fall Time	t_F	90% to 10%, R_L = 3kΩ, C_L = 15pF		10		ns
Duty Cycle	dc_{SYNC}			50		%
DUTY-CYCLE ADJUSTMENT (DADJ)						
DADJ Input Current	I_{DADJ}		190	250	320	μA
DADJ Voltage Range	V_{DADJ}			±2.3		V
Duty-Cycle Adjustment Range	dc	$-2.3V \le V_{DADJ} \le 2.3V$	15		85	%
DADJ Nonlinearity	dc/V_{FADJ}	$-2V \le V_{DADJ} \le 2V$		2	4	%
Change in Output Frequency with DADJ	F_O/V_{DADJ}	$-2V \le V_{DADJ} \le 2V$		±2.5	±8	%
Maximum DADJ Modulating Frequency	F_{DC}			2		MHz
FREQUENCY ADJUSTMENT (FADJ)						
FADJ Input Current	I_{FADJ}		190	250	320	μA
FADJ Voltage Range	V_{FADJ}			±2.4		V
Frequency Sweep Range	F_O	$-2.4V \le V_{FADJ} \le 2.4V$		±70		%
FM Nonlinearity with FADJ	F_O/V_{FADJ}	$-2V \le V_{FADJ} \le 2V$		±0.2		%
Change in Duty Cycle with FADJ	dc/V_{FADJ}	$-2V \le V_{FADJ} \le 2V$		±2		%
Maximum FADJ Modulating Frequency	F_F			2		MHz
VOLTAGE REFERENCE						
Output Voltage	V_{REF}	I_{REF} = 0	2.48	2.50	2.52	V
Temperature Coefficient	V_{REF}/°C			20		ppm/°C
Load Regulation	V_{REF}/I_{REF}	$0mA \le I_{REF} \le 4mA$ (source)		1	2	mV/mA
		$-100μA \le I_{REF} \le 0μA$ (sink)		1	4	
Line Regulation	$V_{REF}/V+$	$4.75V \le V+ \le 5.25V$ (Note 2)		1	2	mV/V
LOGIC INPUTS (A0, A1, PDI)						
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.4			V
Input Current (A0, A1)	I_{IL}, I_{IH}	V_{A0}, V_{A1} = V_{IL}, V_{IH}			±5	μA
Input Current (PDI)	I_{IL}, I_{IH}	V_{PDI} = V_{IL}, V_{IH}			±25	μA
POWER SUPPLY						
Positive Supply Voltage	V+		4.75		5.25	V
SYNC Supply Voltage	DV+		4.75		5.25	V
Negative Supply Voltage	V-		-4.75		-5.25	V
Positive Supply Current	I+			35	45	mA
SYNC Supply Current	I_{DV+}			1	2	mA
Negative Supply Current	I-			45	55	mA

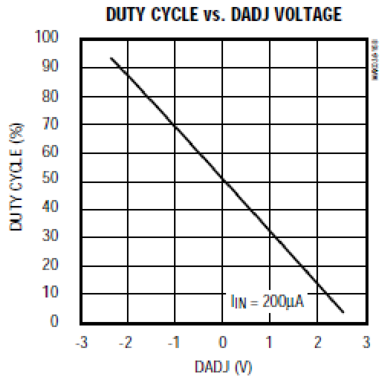
Note 1: Guaranteed by duty-cycle test on square wave.
Note 2: V_{REF} is independent of V-.

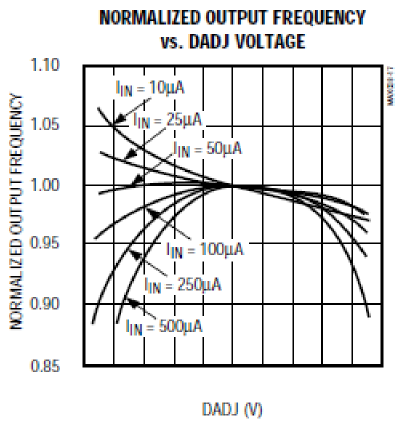
Typical Operating Characteristics

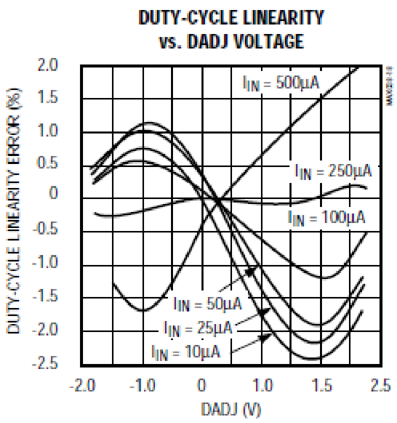
(Circuit of Figure 1, V+ = DV+ = 5V, V- = -5V, $V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO}$ = 0V, R_L = 1kΩ, C_L = 20pF, T_A = +25°C, unless otherwise noted.)







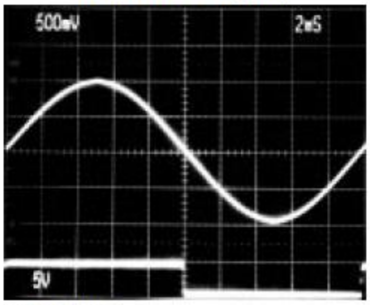




Typical Operating Characteristics (continued)

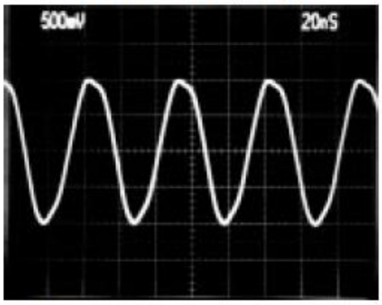
(Circuit of Figure 1, V+ = DV+ = 5V, V- = -5V, $V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO}$ = 0V, R_L = 1kΩ, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

SINE-WAVE OUTPUT (50Hz)



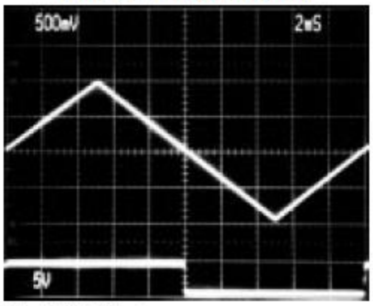
TOP: OUTPUT 50Hz = F_0
BOTTOM: SYNC
I_{IN} = 50µA
C_F = 1µF

SINE-WAVE OUTPUT (20MHz)



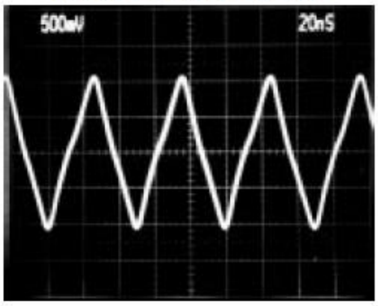
I_{IN} = 400µA
C_F = 20pF

TRIANGLE-WAVE OUTPUT (50Hz)



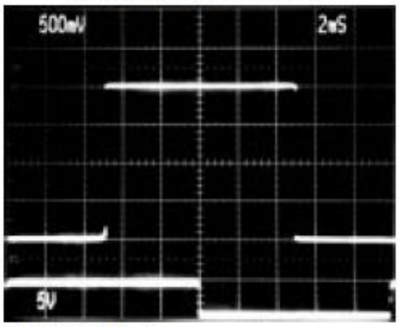
TOP: OUTPUT 50Hz = F_0
BOTTOM: SYNC
I_{IN} = 50µA
C_F = 1µF

TRIANGLE-WAVE OUTPUT (20MHz)



I_{IN} = 400µA
C_F = 20pF

SQUARE-WAVE OUTPUT (50Hz)

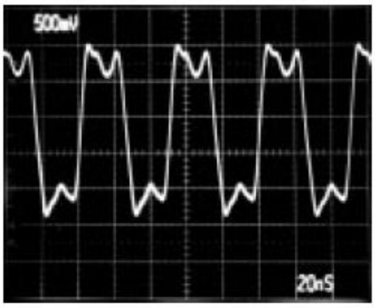


TOP: OUTPUT 50Hz = F_0
BOTTOM: SYNC
I_{IN} = 50µA
C_F = 1µF

Typical Operating Characteristics (continued)

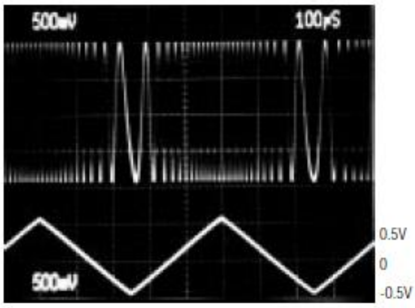
(Circuit of Figure 1, V+ = DV+ = 5V, V- = -5V, $V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO}$ = 0V, R_L = 1kΩ, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

SQUARE-WAVE OUTPUT (20MHz)



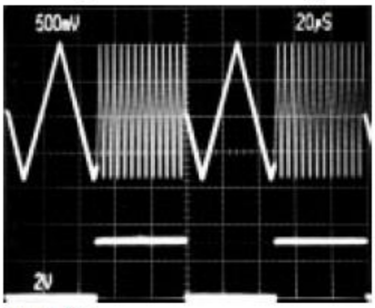
I_{IN} = 400µA
C_F = 20pF

FREQUENCY MODULATION USING FADJ



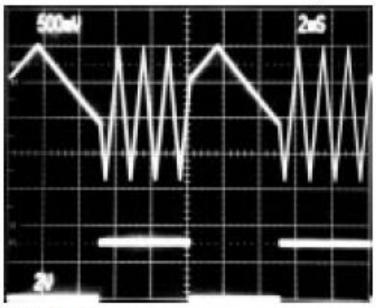
TOP: OUTPUT
BOTTOM: FADJ

FREQUENCY MODULATION USING I_{IN}



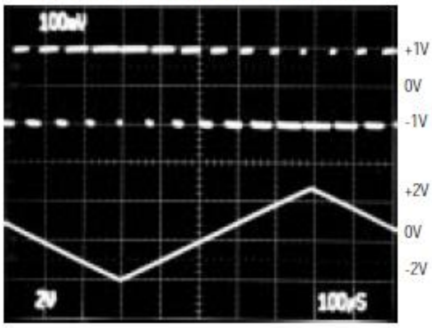
TOP: OUTPUT
BOTTOM: I_{IN}

FREQUENCY MODULATION USING I_{IN}



TOP: OUTPUT
BOTTOM: I_{IN}

PULSE-WIDTH MODULATION USING DADJ

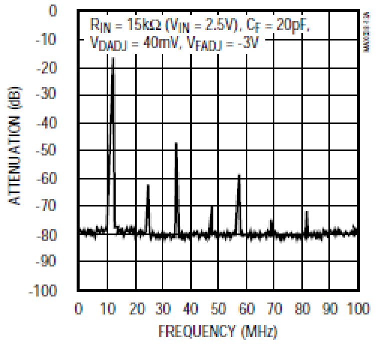


TOP: SQUARE-WAVE OUT, $2V_{P-P}$
BOTTOM: V_{DADJ}, -2V to +2.3V

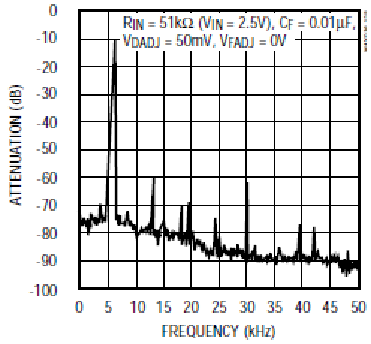
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V+ = DV+ = 5V, V- = -5V, V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO} = 0V, R_L = 1kΩ, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

OUTPUT SPECTRUM, SINE WAVE
(F_O = 11.5MHz)



OUTPUT SPECTRUM, SINE WAVE
(F_O = 5.9kHz)



Pin Description

PIN	NAME	FUNCTION
1	REF	2.50V bandgap voltage reference output
2, 6, 9, 11, 18	GND	Ground*
3	A0	Waveform selection input; TTL/CMOS compatible
4	A1	Waveform selection input; TTL/CMOS compatible
5	COSC	External capacitor connection
7	DADJ	Duty-cycle adjust input
8	FADJ	Frequency adjust input
10	IIN	Current input for frequency control
12	PDO	Phase detector output. Connect to GND if phase detector is not used.
13	PDI	Phase detector reference clock input. Connect to GND if phase detector is not used.
14	SYNC	TTL/CMOS-compatible output, referenced between DGND and DV+. Permits the internal oscillator to be synchronized with an external signal. Leave open if unused.
15	DGND	Digital ground
16	DV+	Digital +5V supply input. Can be left open if SYNC is not used.
17	V+	+5V supply input
19	OUT	Sine, square, or triangle output
20	V-	-5V supply input

**The five GND pins are not internally connected. Connect all five GND pins to a quiet ground close to the device. A ground plane is recommended (see Layout Considerations).*

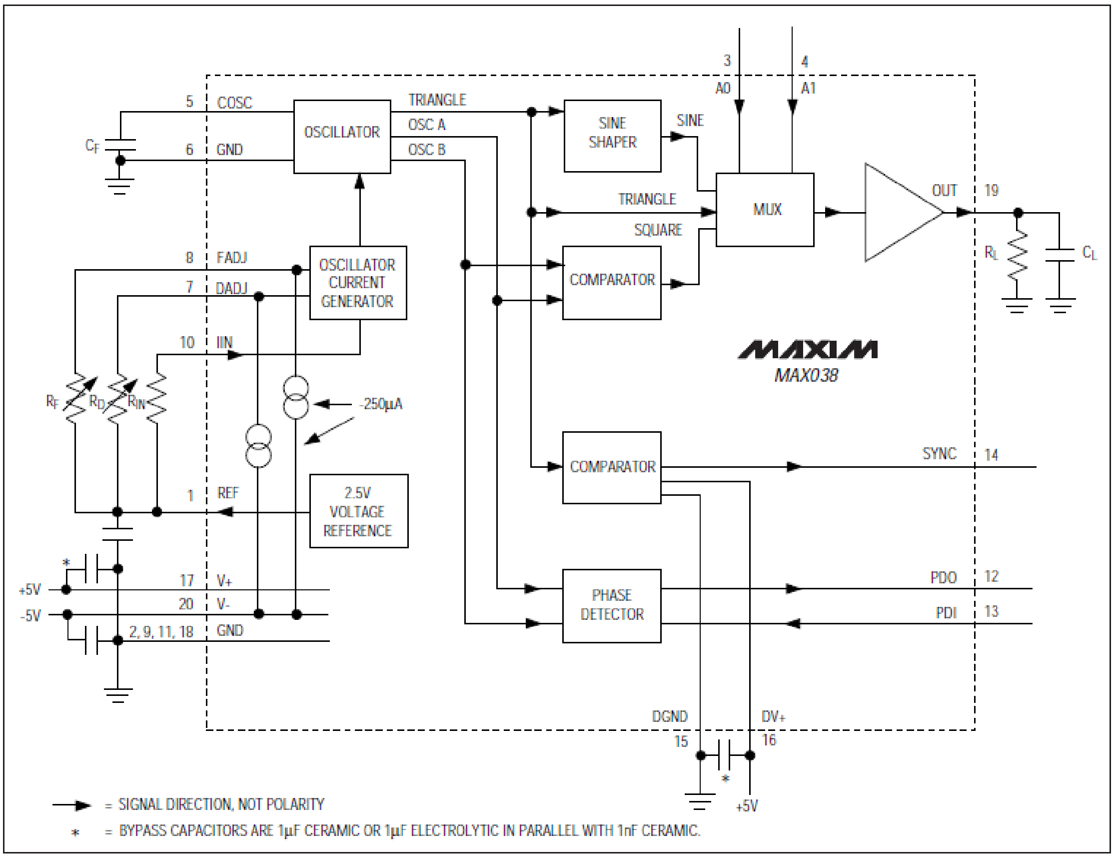


Figure 1. Block Diagram and Basic Operating Circuit

Detailed Description

The MAX038 is a high-frequency function generator that produces low-distortion sine, triangle, sawtooth, or square (pulse) waveforms at frequencies from less than 1Hz to 20MHz or more, using a minimum of external components. Frequency and duty cycle can be independently controlled by programming the current, voltage, or resistance. The desired output waveform is selected under logic control by setting the appropriate code at the A0 and A1 inputs. A SYNC output and phase detector are included to simplify designs requiring tracking to an external signal source.

The MAX038 operates with ±5V ±5% power supplies. The basic oscillator is a relaxation type that operates by alternately charging and discharging a capacitor, C_F, with constant currents, simultaneously producing a triangle wave and a square wave (Figure 1). The charging and discharging currents are controlled by the current flowing into IIN, and are modulated by the voltages applied to FADJ and DADJ. The current into IIN can be varied from 2µA to 750µA, producing more than two decades of frequency for any value of C_F. Applying ±2.4V to FADJ changes the nominal frequency (with V_{FADJ} = 0V) by ±70%; this procedure can be used for fine control.

Duty cycle (the percentage of time that the output waveform is positive) can be controlled from 10% to 90% by applying ±2.3V to DADJ. This voltage changes the C_F charging and discharging current ratio while maintaining nearly constant frequency.

A stable 2.5V reference voltage, REF, allows simple determination of IIN, FADJ, or DADJ with fixed resistors, and permits adjustable operation when potentiometers are connected from each of these inputs to REF. FADJ and/or DADJ can be grounded, producing the nominal frequency with a 50% duty cycle.

The output frequency is inversely proportional to capacitor C_F. C_F values can be selected to produce frequencies above 20MHz.

A sine-shaping circuit converts the oscillator triangle wave into a low-distortion sine wave with constant amplitude. The triangle, square, and sine waves are input to a multiplexer. Two address lines, A0 and A1, control which of the three waveforms is selected. The output amplifier produces a constant $2V_{P-P}$ amplitude (±1V), regardless of wave shape or frequency.

The triangle wave is also sent to a comparator that produces a high-speed square-wave SYNC waveform that can be used to synchronize other oscillators. The SYNC circuit has separate power-supply leads and can be disabled.

Two other phase-quadrature square waves are generated in the basic oscillator and sent to one side of an "exclusive-OR" phase detector. The other side of the phase-detector input (PDI) can be connected to an external oscillator. The phase-detector output (PDO) is a current source that can be connected directly to FADJ to synchronize the MAX038 with the external oscillator.

Waveform Selection

The MAX038 can produce either sine, square, or triangle waveforms. The TTL/CMOS-logic address pins (A0 and A1) set the waveform, as shown below:

A0	A1	WAVEFORM
X	1	Sine wave
0	0	Square wave
1	0	Triangle wave

X = Don't care

Waveform switching can be done at any time, without regard to the phase of the output. Switching occurs within 0.3µs, but there may be a small transient in the output waveform that lasts 0.5µs.

Waveform Timing

Output Frequency

The output frequency is determined by the current injected into the IIN pin, the COSC capacitance (to ground), and the voltage on the FADJ pin. When V_{FADJ} = 0V, the fundamental output frequency (F_O) is given by the formula:

$$F_O\,(MHz) = I_{IN}\,(\mu A) \div C_F\,(pF) \qquad [1]$$

The period (t_O) is:

$$t_O\,(\mu s) = C_F\,(pF) \div I_{IN}\,(\mu A) \qquad [2]$$

where:

I_{IN} = current injected into IIN (between 2µA and 750µA)

C_F = capacitance connected to COSC and GND (20pF to >100µF).

For example:

0.5MHz = 100µA ÷ 200pF

and

2µs = 200pF ÷ 100µA

Optimum performance is achieved with I_{IN} between 10µA and 400µA, although linearity is good with I_{IN} between 2µA and 750µA. Current levels outside of this range are not recommended. For fixed-frequency operation, set I_{IN} to approximately 100µA and select a suitable capacitor value. This current produces the lowest temperature coefficient, and produces the lowest frequency shift when varying the duty cycle.

The capacitance can range from 20pF to more than 100µF, but stray circuit capacitance must be minimized by using short traces. Surround the COSC pin and the trace leading to it with a ground plane to minimize coupling of extraneous signals to this node. Oscillation above 20MHz is possible, but waveform distortion increases under these conditions. The low frequency limit is set by the leakage of the COSC capacitor and by the required accuracy of the output frequency. Lowest frequency operation with good accuracy is usually achieved with 10µF or greater non-polarized capacitors.

An internal closed-loop amplifier forces IIN to virtual ground, with an input offset voltage less than ±2mV. IIN may be driven with either a current source (I_{IN}), or a voltage (V_{IN}) in series with a resistor (R_{IN}). (A resistor between REF and IIN provides a convenient method of generating I_{IN}: $I_{IN} = V_{REF}/R_{IN}$.) When using a voltage in series with a resistor, the formula for the oscillator frequency is:

$$F_O\,(MHz) = V_{IN} \div [R_{IN} \times C_F\,(pF)] \qquad [3]$$

and:

$$t_O\,(\mu s) = C_F\,(pF) \times R_{IN} \div V_{IN} \qquad [4]$$

When the MAX038's frequency is controlled by a voltage source (V_{IN}) in series with a fixed resistor (R_{IN}), the output frequency is a direct function of V_{IN} as shown in the above equations. Varying V_{IN} modulates the oscillator frequency. For example, using a 10kΩ resistor for R_{IN} and sweeping V_{IN} from 20mV to 7.5V produces large frequency deviations (up to 375:1). Select R_{IN} so that I_{IN} stays within the 2μA to 750μA range. The bandwidth of the IIN control amplifier, which limits the modulating signal's highest frequency, is typically 2MHz.

IIN can be used as a summing point to add or subtract currents from several sources. This allows the output frequency to be a function of the sum of several variables. As V_{IN} approaches 0V, the I_{IN} error increases due to the offset voltage of IIN.

Output frequency will be offset 1% from its final value for 10 seconds after power-up.

FADJ Input

The output frequency can be modulated by FADJ, which is intended principally for fine frequency control, usually inside phase-locked loops. Once the fundamental, or center frequency (F_0) is set by I_{IN}, it may be changed further by setting FADJ to a voltage other than 0V. This voltage can vary from -2.4V to +2.4V, causing the output frequency to vary from 1.7 to 0.30 times the value when FADJ is 0V (F_0 ±70%). Voltages beyond ±2.4V can cause instability or cause the frequency change to reverse slope.

The voltage on FADJ required to cause the output to deviate from F_0 by D_X (expressed in %) is given by the formula:

$$V_{FADJ} = -0.0343 \times D_X \qquad [5]$$

where V_{FADJ}, the voltage on FADJ, is between -2.4V and +2.4V.

Note: While I_{IN} is directly proportional to the fundamental, or center frequency (F_0), V_{FADJ} is linearly related to % deviation from F_0. V_{FADJ} goes to either side of 0V, corresponding to plus and minus deviation.

The voltage on FADJ for any frequency is given by the formula:

$$V_{FADJ} = (F_0 - F_X) \div (0.2915 \times F_0) \qquad [6]$$

where:

F_X = output frequency

F_0 = frequency when V_{FADJ} = 0V.

Likewise, for period calculations:

$$V_{FADJ} = 3.43 \times (t_X - t_0) \div t_X \qquad [7]$$

where:

t_X = output period

t_0 = period when V_{FADJ} = 0V.

Conversely, if V_{FADJ} is known, the frequency is given by:

$$F_X = F_0 \times (1 - [0.2915 \times V_{FADJ}]) \qquad [8]$$

and the period (t_X) is:

$$t_X = t_0 \div (1 - [0.2915 \times V_{FADJ}]) \qquad [9]$$

Programming FADJ

FADJ has a 250μA constant current sink to V- that must be furnished by the voltage source. The source is usually an op-amp output, and the temperature coefficient of the current sink becomes unimportant. For manual adjustment of the deviation, a variable resistor can be used to set V_{FADJ}, but then the 250μA current sink's temperature coefficient becomes significant. Since external resistors cannot match the internal temperature-coefficient curve, using external resistors to program V_{FADJ} is intended only for manual operation, when the operator can correct for any errors. This restriction does not apply when V_{FADJ} is a true voltage source.

A variable resistor, R_F, connected between REF (+2.5V) and FADJ provides a convenient means of manually setting the frequency deviation. The resistance value (R_F) is:

$$R_F = (V_{REF} - V_{FADJ}) \div 250\mu A \qquad [10]$$

V_{REF} and V_{FADJ} are signed numbers, so use correct algebraic convention. For example, if V_{FADJ} is -2.0V (+58.3% deviation), the formula becomes:

$$R_F = (+2.5V - (-2.0V)) \div 250\mu A$$
$$= (4.5V) \div 250\mu A$$
$$= 18k\Omega$$

Disabling FADJ

The FADJ circuit adds a small temperature coefficient to the output frequency. For critical open-loop applications, it can be turned off by connecting FADJ to GND (not REF) through a 12kΩ resistor (R1 in Figure 2). The -250μA current sink at FADJ causes -3V to be developed across this resistor, producing two results. First, the FADJ circuit remains in its linear region, but disconnects itself from the main oscillator, improving temperature stability. Second, the oscillator frequency doubles. If FADJ is turned off in this manner, be sure to correct equations 1-4 and 6-9 above, and 12 and 14 below by doubling F_0 or halving t_0. Although this method doubles the normal output frequency, it does not double the upper frequency limit. Do not operate FADJ open circuit or with voltages more negative than -3.5V. Doing so may cause transistor saturation inside the IC, leading to unwanted changes in frequency and duty cycle.

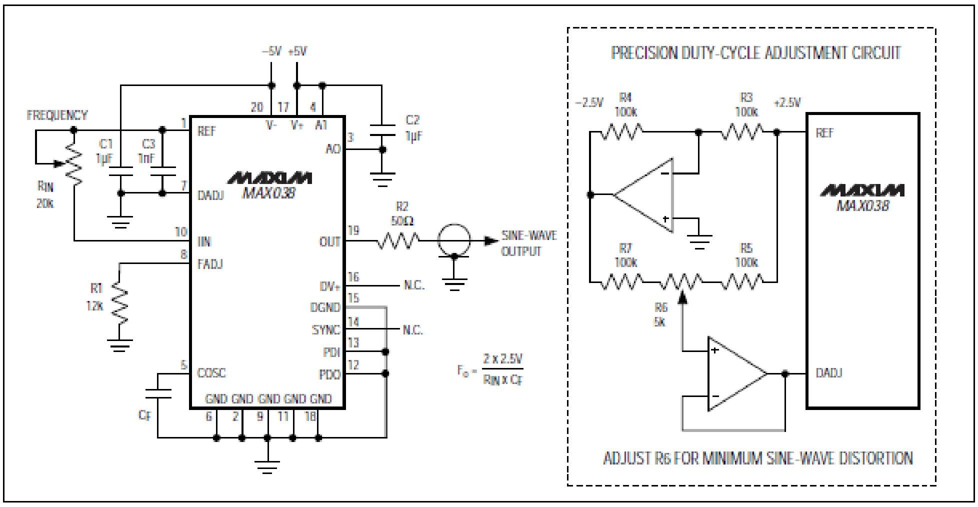


Figure 2. Operating Circuit with Sine-Wave Output and 50% Duty Cycle; SYNC and FADJ Disabled

With FADJ disabled, the output frequency can still be changed by modulating I_{IN}.

Swept Frequency Operation

The output frequency can be swept by applying a varying signal to IIN or FADJ. IIN has a wider range, slightly slower response, lower temperature coefficient, and requires a single polarity current source. FADJ may be used when the swept range is less than ±70% of the center frequency, and it is suitable for phase-locked loops and other low-deviation, high-accuracy closed-loop controls. It uses a sweeping voltage symmetrical about ground.

Connecting a resistive network between REF, the voltage source, and FADJ or IIN is a convenient means of offsetting the sweep voltage.

Duty Cycle

The voltage on DADJ controls the waveform duty cycle (defined as the percentage of time that the output waveform is positive). Normally, V_{DADJ} = 0V, and the duty cycle is 50% (Figure 2). Varying this voltage from +2.3V to -2.3V causes the output duty cycle to vary from 15% to 85%, about -15% per volt. Voltages beyond ±2.3V can shift the output frequency and/or cause instability.

DADJ can be used to reduce the sine-wave distortion. The unadjusted duty cycle (V_{DADJ} = 0V) is 50% ±2%; any deviation from exactly 50% causes even order harmonics to be generated. By applying a small adjustable voltage (typically less than ±100mV) to V_{DADJ}, exact symmetry can be attained and the distortion can be minimized (see Figure 2).

The voltage on DADJ needed to produce a specific duty cycle is given by the formula:

$$V_{DADJ} = (50\% - dc) \times 0.0575 \qquad [11]$$

or:

$$V_{DADJ} = (0.5 - [t_{ON} \div t_o]) \times 5.75 \qquad [12]$$

where:

V_{DADJ} = DADJ voltage (observe the polarity)

dc = duty cycle (in %)

t_{ON} = ON (positive) time

t_o = waveform period.

Conversely, if V_{DADJ} is known, the duty cycle and ON time are given by:

$$dc = 50\% - (V_{DADJ} \times 17.4) \qquad [13]$$

$$t_{ON} = t_o \times (0.5 - [V_{DADJ} \times 0.174]) \qquad [14]$$

Programming DADJ

DADJ is similar to FADJ; it has a 250µA constant current sink to V- that must be furnished by the voltage source. The source is usually an op-amp output, and the temperature coefficient of the current sink becomes unimportant. For manual adjustment of the duty cycle, a variable resistor can be used to set V_{DADJ}, but then the 250µA current sink's temperature coefficient becomes significant. Since external resistors cannot match the internal temperature-coefficient curve, using external resistors to program V_{DADJ} is intended only for manual operation, when the operator can correct for any errors. This restriction does not apply when V_{DADJ} is a true voltage source.

A variable resistor, R_D, connected between REF (+2.5V) and DADJ provides a convenient means of manually setting the duty cycle. The resistance value (R_D) is:

$$R_D = (V_{REF} - V_{DADJ}) \div 250\mu A \qquad [15]$$

Note that both V_{REF} and V_{DADJ} are signed values, so observe correct algebraic convention. For example, if V_{DADJ} is -1.5V (23% duty cycle), the formula becomes:

$$R_D = (+2.5V - (-1.5V)) \div 250\mu A$$
$$= (4.0V) \div 250\mu A = 16k\Omega$$

Varying the duty cycle in the range 15% to 85% has minimal effect on the output frequency—typically less than 2% when $25\mu A < I_{IN} < 250\mu A$. The DADJ circuit is wideband, and can be modulated at up to 2MHz (see photos, *Typical Operating Characteristics*).

Output

The output amplitude is fixed at $2V_{P-P}$, symmetrical around ground, for all output waveforms. OUT has an output resistance of under 0.1Ω, and can drive ±20mA with up to a 50pF load. Isolate higher output capacitance from OUT with a resistor (typically 50Ω) or buffer amplifier.

Reference Voltage

REF is a stable 2.50V bandgap voltage reference capable of sourcing 4mA or sinking 100µA. It is principally used to furnish a stable current to IIN or to bias DADJ and FADJ. It can also be used for other applications external to the MAX038. Bypass REF with 100nF to minimize noise.

Selecting Resistors and Capacitors

The MAX038 produces a stable output frequency over time and temperature, but the capacitor and resistors that determine frequency can degrade performance if they are not carefully chosen. Resistors should be metal film, 1% or better. Capacitors should be chosen for low temperature coefficient over the whole temperature range. NPO ceramics are usually satisfactory.

The voltage on COSC is a triangle wave that varies between 0V and -1V. Polarized capacitors are generally not recommended (because of their outrageous temperature dependence and leakage currents), but if they are used, the negative terminal should be connected to COSC and the positive terminal to GND. Large-value capacitors, necessary for very low frequencies, should be chosen with care, since potentially large leakage currents and high dielectric absorption can interfere with the orderly charge and discharge of C_F. If possible, for a given frequency, use lower IIN currents to reduce the size of the capacitor.

SYNC Output

SYNC is a TTL/CMOS-compatible output that can be used to synchronize external circuits. The SYNC output is a square wave whose rising edge coincides with the output rising sine or triangle wave as it crosses through 0V. When the square wave is selected, the rising edge of SYNC occurs in the middle of the positive half of the output square wave, effectively 90° ahead of the output. The SYNC duty cycle is fixed at 50% and is independent of the DADJ control.

Because SYNC is a very-high-speed TTL output, the high-speed transient currents in DGND and DV+ can radiate energy into the output circuit, causing a narrow spike in the output waveform. (This spike is difficult to see with oscilloscopes having less than 100MHz bandwidth). The inductance and capacitance of IC sockets tend to amplify this effect, so sockets are not recommended when SYNC is on. SYNC is powered from separate ground and supply pins (DGND and DV+), and it can be turned off by making DV+ open circuit. If synchronization of external circuits is not used, turning off SYNC by DV+ opening eliminates the spike.

Phase Detectors

Internal Phase Detector

The MAX038 contains a TTL/CMOS phase detector that can be used in a phase-locked loop (PLL) to synchronize its output to an external signal (Figure 3). The external source is connected to the phase-detector input (PDI) and the phase-detector output is taken from PDO. PDO is the output of an exclusive-OR gate, and produces a rectangular current waveform at the MAX038 output frequency, even with PDI grounded. PDO is normally connected to FADJ and a resistor, R_{PD}, and a capacitor C_{PD}, to GND. R_{PD} sets the gain of the phase detector, while the capacitor attenuates high-frequency components and forms a pole in the phase-locked loop filter.

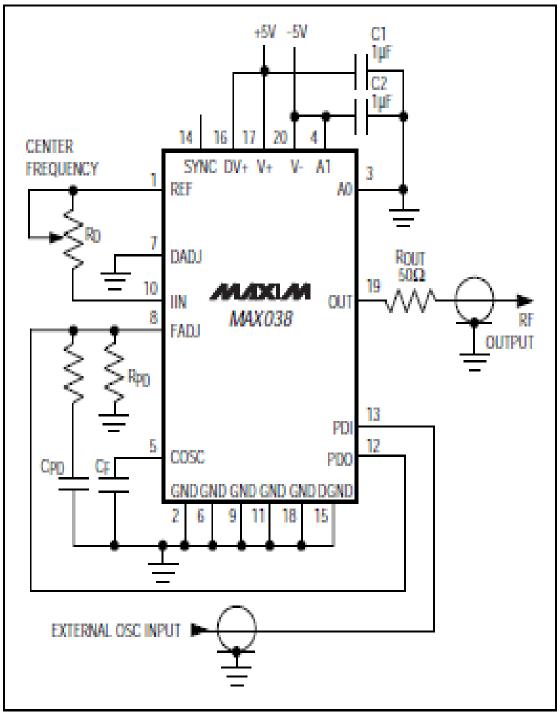


Figure 3. Phase-Locked Loop Using Internal Phase Detector

PDO is a rectangular current-pulse train, alternating between 0µA and 500µA. It has a 50% duty cycle when the MAX038 output and PDI are in phase-quadrature (90° out of phase). The duty cycle approaches 100% as the phase difference approaches 180° and conversely, approaches 0% as the phase difference approaches 0°. The gain of the phase detector (K_D) can be expressed as:

$$K_D = 0.318 \times R_{PD} \text{ (volts/radian)} \quad [16]$$

where R_{PD} = phase-detector gain-setting resistor.

When the loop is in lock, the input signals to the phase detector are in approximate phase quadrature, the duty cycle is 50%, and the average current at PDO is 250µA (the current sink of FADJ). This current is divided between FADJ and R_{PD}; 250µA always goes into FADJ and any difference current is developed across R_{PD}, creating V_{FADJ} (both polarities). For example, as the phase difference increases, PDO duty cycle increases, the average current increases, and the voltage on R_{PD} (and V_{FADJ}) becomes more positive. This in turn decreases the oscillator frequency, reducing the phase difference, thus maintaining phase lock. The higher R_{PD} is, the greater V_{FADJ} is for a given phase difference; in other words, the greater the loop gain, the less the capture range. The current from PDO must also charge C_{PD}, so the rate at which V_{FADJ} changes (the loop bandwidth) is inversely proportional to C_{PD}.

The phase error (deviation from phase quadrature) depends on the open-loop gain of the PLL and the initial frequency deviation of the oscillator from the external signal source. The oscillator conversion gain (K_O) is:

$$K_O = \Delta\omega_0 \div \Delta V_{FADJ} \quad [17]$$

which, from equation [6] is:

$$K_O = 3.43 \times \omega_0 \text{ (radians/sec)} \quad [18]$$

The loop gain of the PLL system (K_V) is:

$$K_V = K_D \times K_O \quad [19]$$

where:

K_D = detector gain

K_O = oscillator gain.

With a loop filter having a response F(s), the open-loop transfer function, T(s), is:

$$T(s) = K_D \times K_O \times F(s) \div s \quad [20]$$

Using linear feedback analysis techniques, the closed-loop transfer characteristic, H(s), can be related to the open-loop transfer function as follows:

$$H(s) = T(s) \div [1 + T(s)] \quad [21]$$

The transient performance and the frequency response of the PLL depends on the choice of the filter characteristic, F(s).

When the MAX038 internal phase detector is not used, PDI and PDO should be connected to GND.

External Phase Detectors

External phase detectors may be used instead of the internal phase detector. The external phase detector shown in Figure 4 duplicates the action of the MAX038's internal phase detector, but the optional ÷N circuit can be placed between the SYNC output and the phase detector in applications requiring synchronizing to an exact multiple of the external oscillator. The resistor network consisting of R4, R5, and R6 sets the sync range, while capacitor C4 sets the capture range. Note that this type of phase detector (with or without the ÷N circuit) locks onto harmonics of the external oscillator as well as the fundamental. With no external oscillator input, this circuit can be unpredictable, depending on the state of the external input DC level.

Figure 4 shows a frequency phase detector that locks onto only the fundamental of the external oscillator. With no external oscillator input, the output of the frequency phase detector is a positive DC voltage, and the oscillations are at the lowest frequency as set by R4, R5, and R6.

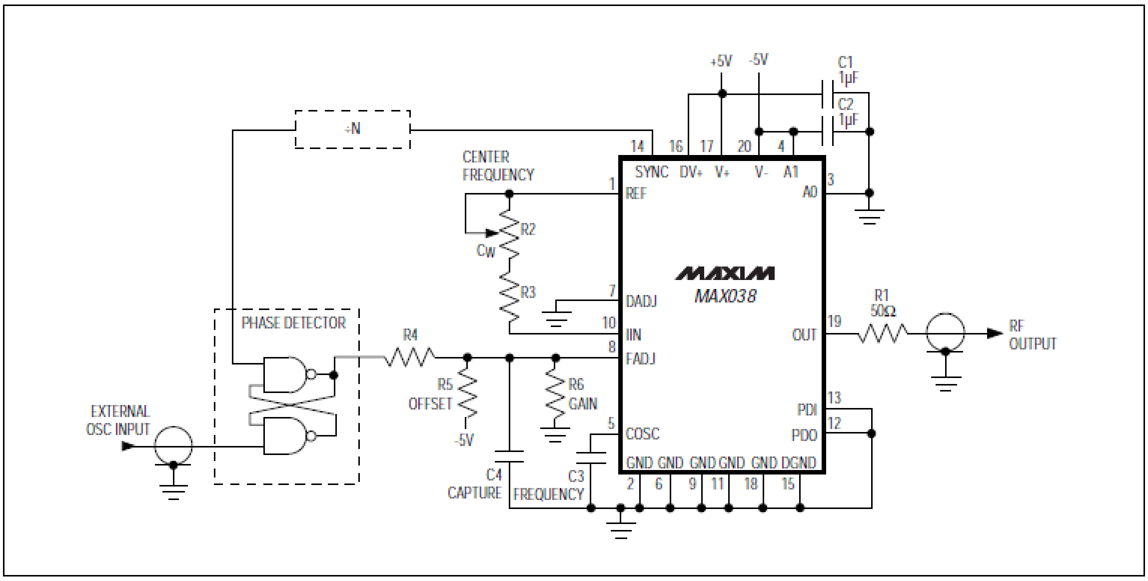


Figure 4. Phase-Locked Loop Using External Phase Detector

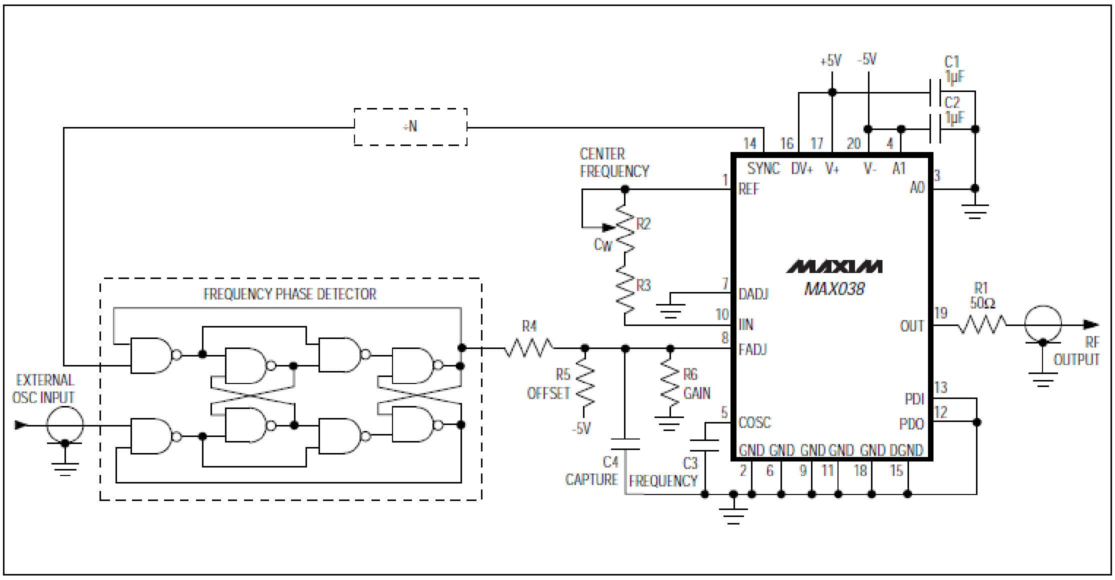


Figure 5. Phase-Locked Loop Using External Frequency Phase Detector

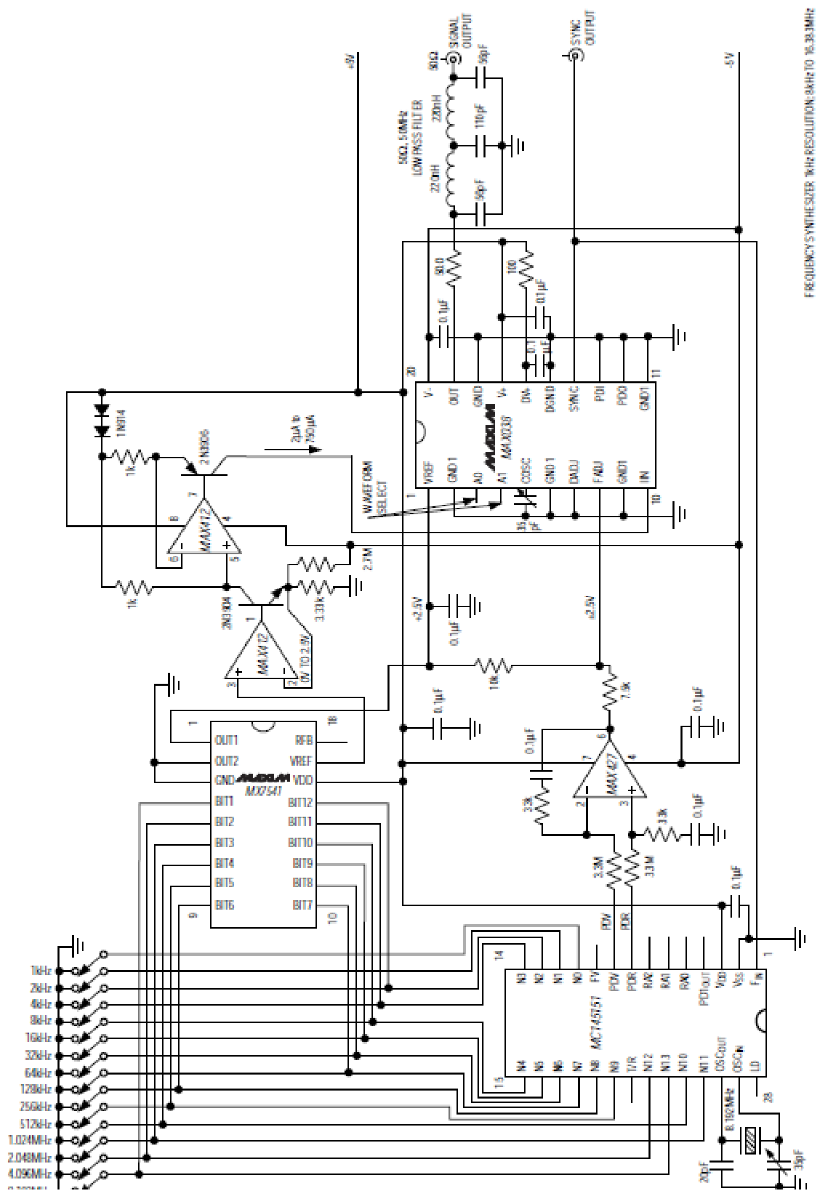


Figure 6. Crystal-Controlled, Digitally Programmed Frequency Synthesizer—8kHz to 16MHz with 1kHz Resolution

Layout Considerations

Realizing the full performance of the MAX038 requires careful attention to power-supply bypassing and board layout. Use a low-impedance ground plane, and connect all five GND pins directly to it. Bypass V+ and V- directly to the ground plane with 1µF ceramic capacitors or 1µF tantalum capacitors in parallel with 1nF ceramics. Keep capacitor leads short (especially with the 1nF ceramics) to minimize series inductance.

If SYNC is used, DV+ must be connected to V+, DGND must be connected to the ground plane, and a second 1nF ceramic should be connected as close as possible between DV+ and DGND (pins 16 and 15). It is not necessary to use a separate supply or run separate traces to DV+. If SYNC is disabled, leave DV+ open. Do not open DGND.

Minimize the trace area around COSC (and the ground plane area under COSC) to reduce parasitic capacitance, and surround this trace with ground to prevent coupling with other signals. Take similar precautions with DADJ, FADJ, and IIN. Place C_F so its connection to the ground plane is close to pin 6 (GND).

Applications Information

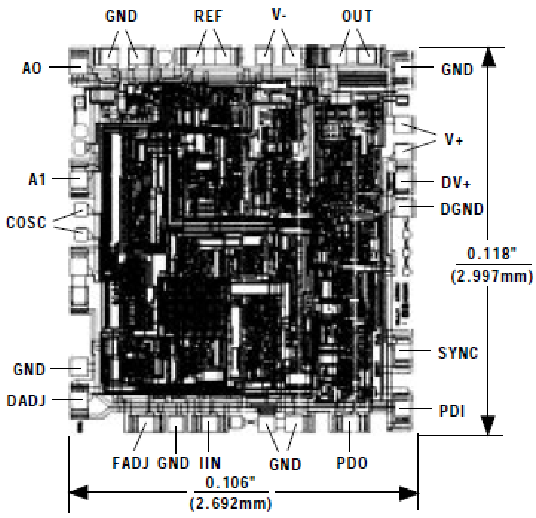
Frequency Synthesizer

Figure 6 shows a frequency synthesizer that produces accurate and stable sine, square, or triangle waves with a frequency range of 8kHz to 16.383MHz in 1kHz increments. A Motorola MC145151 provides the crystal-controlled oscillator, the ÷N circuit, and a high-speed phase detector. The manual switches set the output frequency; opening any switch increases the output frequency. Each switch controls both the ÷N output and an MX7541 12-bit DAC, whose output is converted to a current by using both halves of the MAX412 op amp. This current goes to the MAX038 IIN pin, setting its coarse frequency over a very wide range.

Fine frequency control (and phase lock) is achieved from the MC145151 phase detector through the differential amplifier and lowpass filter, U5. The phase detector compares the ÷N output with the MAX038 SYNC output and sends differential phase information to U5. U5's single-ended output is summed with an offset into the FADJ input. (Using the DAC and the IIN pin for coarse frequency control allows the FADJ pin to have very fine control with reasonably fast response to switch changes.)

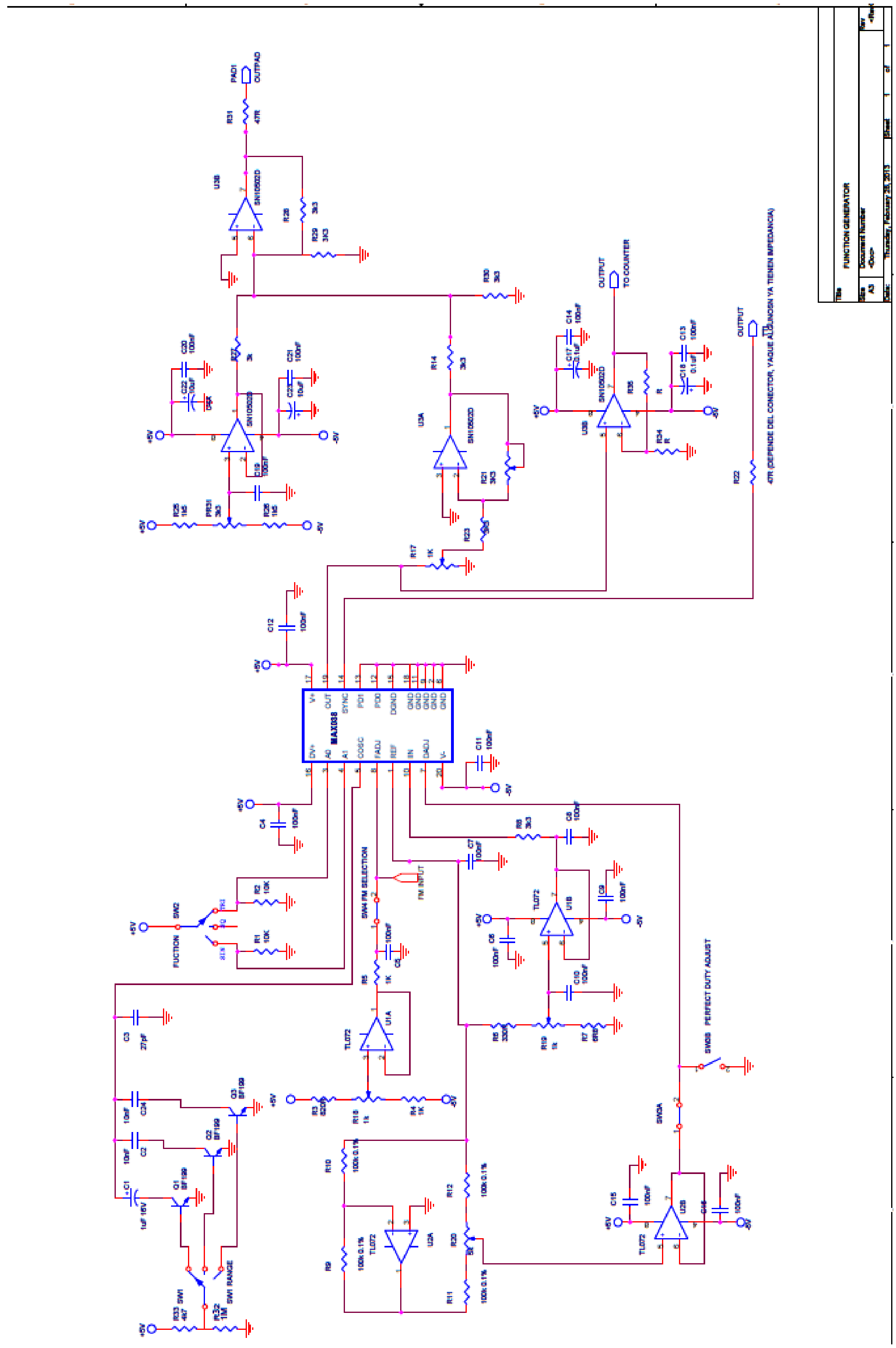
A 50MHz, 50Ω lowpass filter in the output allows passage of 16MHz square waves and triangle waves with reasonable fidelity, while stopping high-frequency noise generated by the ÷N circuit.

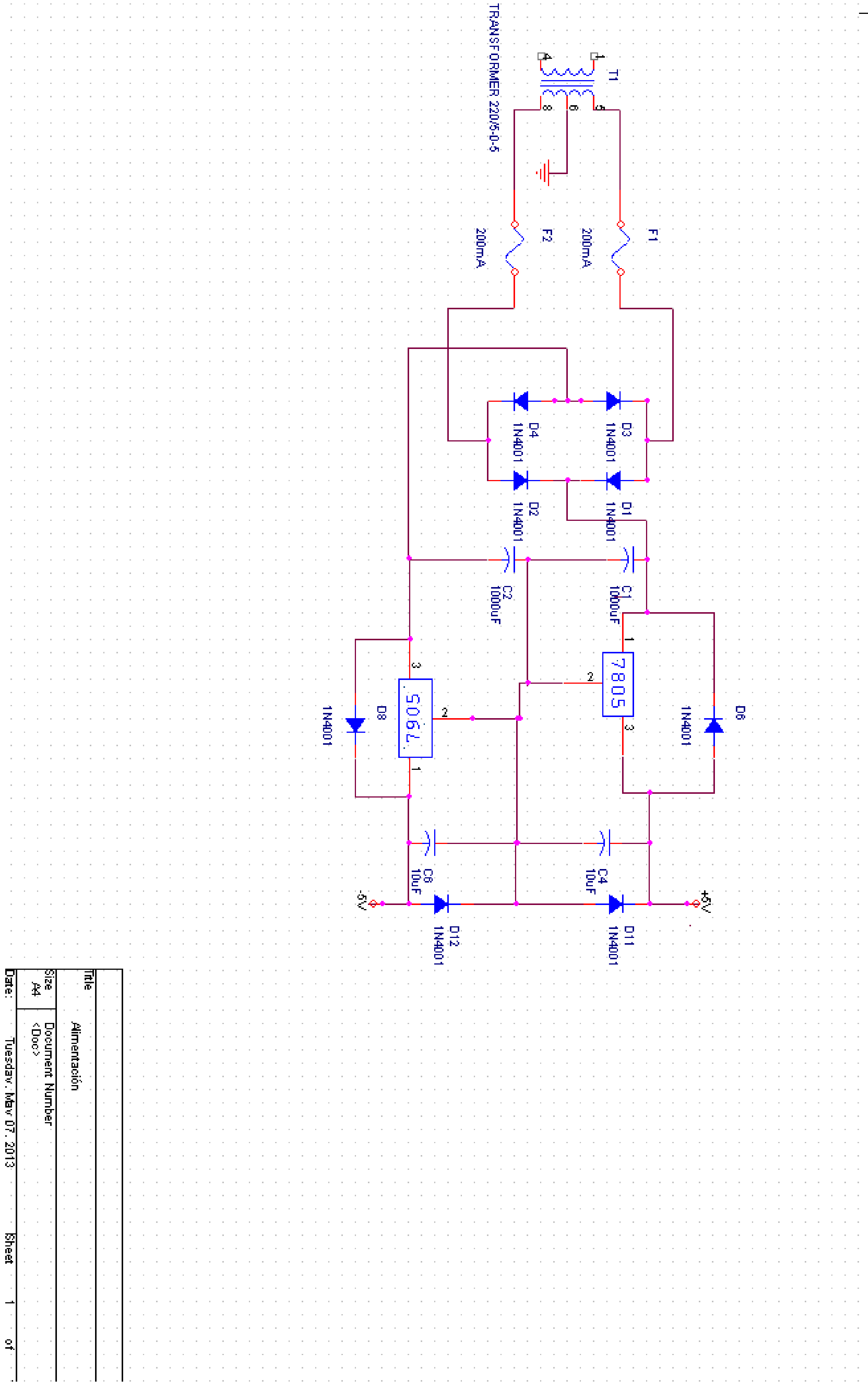
Chip Topography



TRANSISTOR COUNT: 855
SUBSTRATE CONNECTED TO GND

SCHEMATICS

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F2
200mA
D1
1N4001
D2
1N4001
D3
1N4001
D4
1N4001
C1
1000uF
C2
1000uF
7805
7905
D6
1N4001
D8
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C4
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+5V
-5V
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Alimentación
Size
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Date: Tuesday, May 07, 2013
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