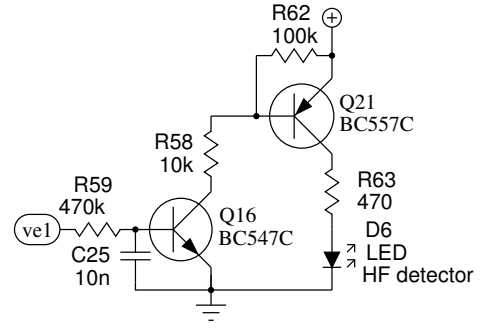
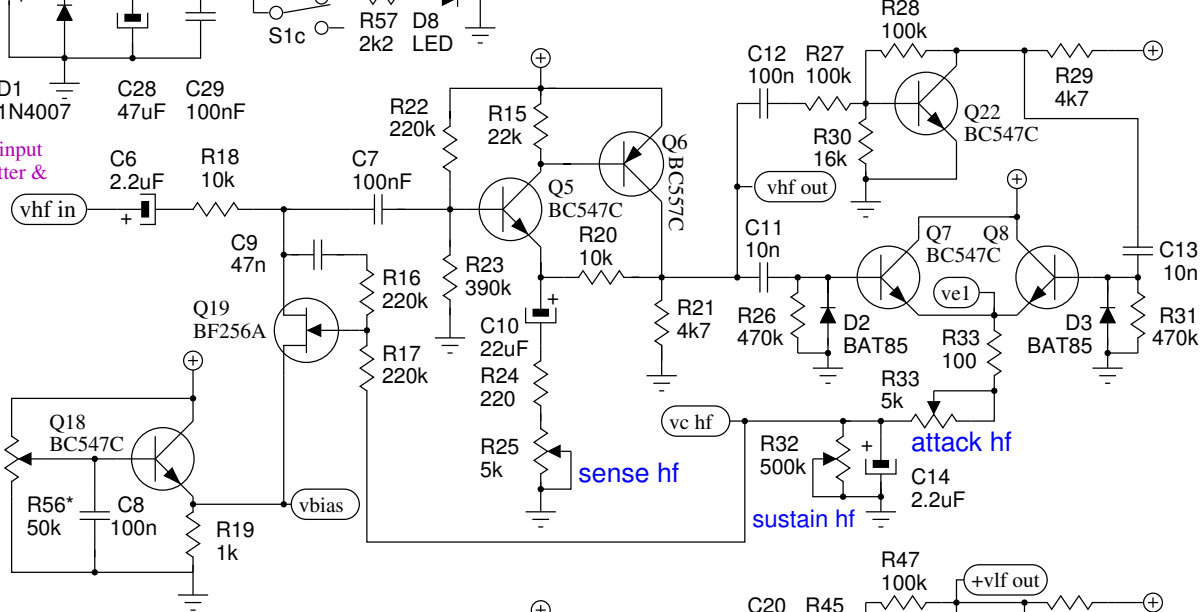


\*adjust R3 so 4Vpp sine input is undistorted at Q1 emitter & collector.



\* adjust R56 so FETs slightly in pinchoff

