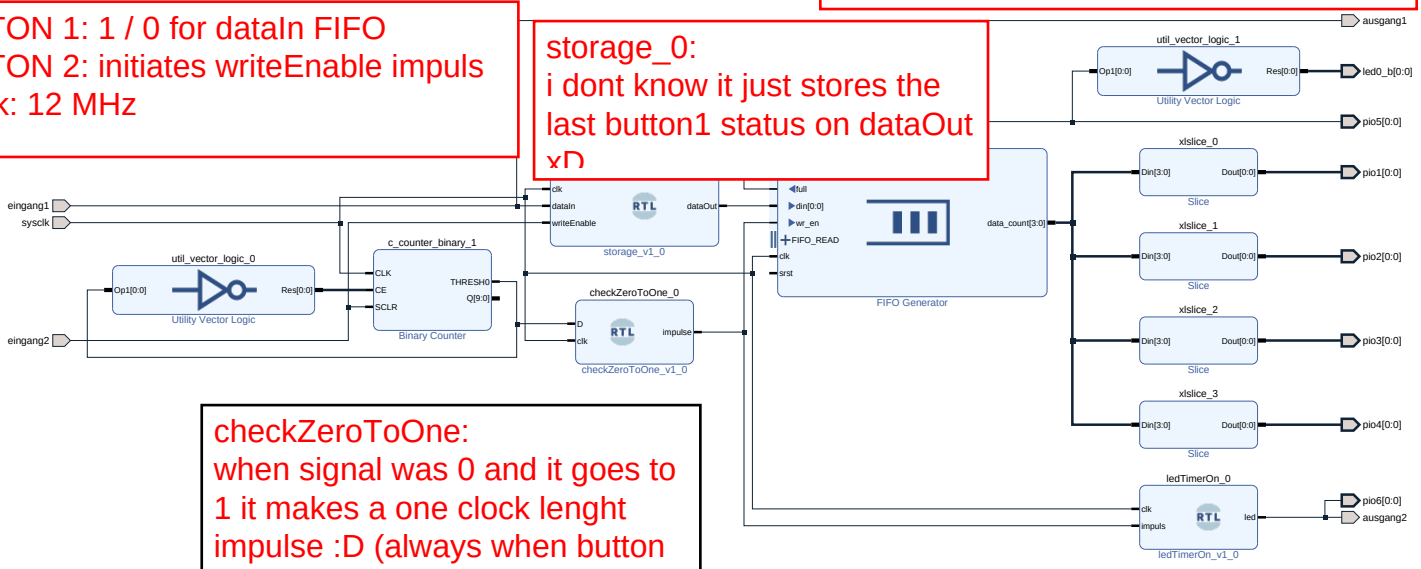
THIS IS A RANDOM TEST BLOCK DESIGN - BUT IT WORKS!

When FIFO is full (16 Bits) then full will go HIGH
-- the normal PIO5 - LED will shine
the rgb - BLUE needs a LOW to shine (NOT-BLOCK)

BUTTON 1: 1 / 0 for dataIn FIFO
BUTTON 2: initiates writeEnable impuls
sysclk: 12 MHz

storage_0:
i dont know it just stores the last button1 status on dataOut xD



checkZeroToOne:
when signal was 0 and it goes to 1 it makes a one clock lenght impulse :D (always when button pressed)

counter_binary_1
(i didnt check the simulation right:)
it counts up with CLK which is there since beginning
THRESH0 is low first so the CE entry will be high first
When THRESH0 (something like 2^10) is reached it gets HIGH! so CE entry gets LOW! Which disables the counter!
It stops
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Only when it is resettet by SCLR the threshold is not reached and THRESH0 goes to LOW and so CE entry is one again.
SCLR can set the counter to 0 -> only when BUTTON2 is pressed!
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ledTimerOn_0:
when the impulse comes it sets the output for around 1 second to HIGH
PIO6 and AUSGANG2 - LEDS will be on for 2 Seconds :D

the data_count[3:0] shows how much data are stored since beginning... the 4 connected LEDs are connected to this bus and you will a binary counting from 0 to 15
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the 0 doesnt show up xD maybe because the counter gives an impuls directly at the beginning