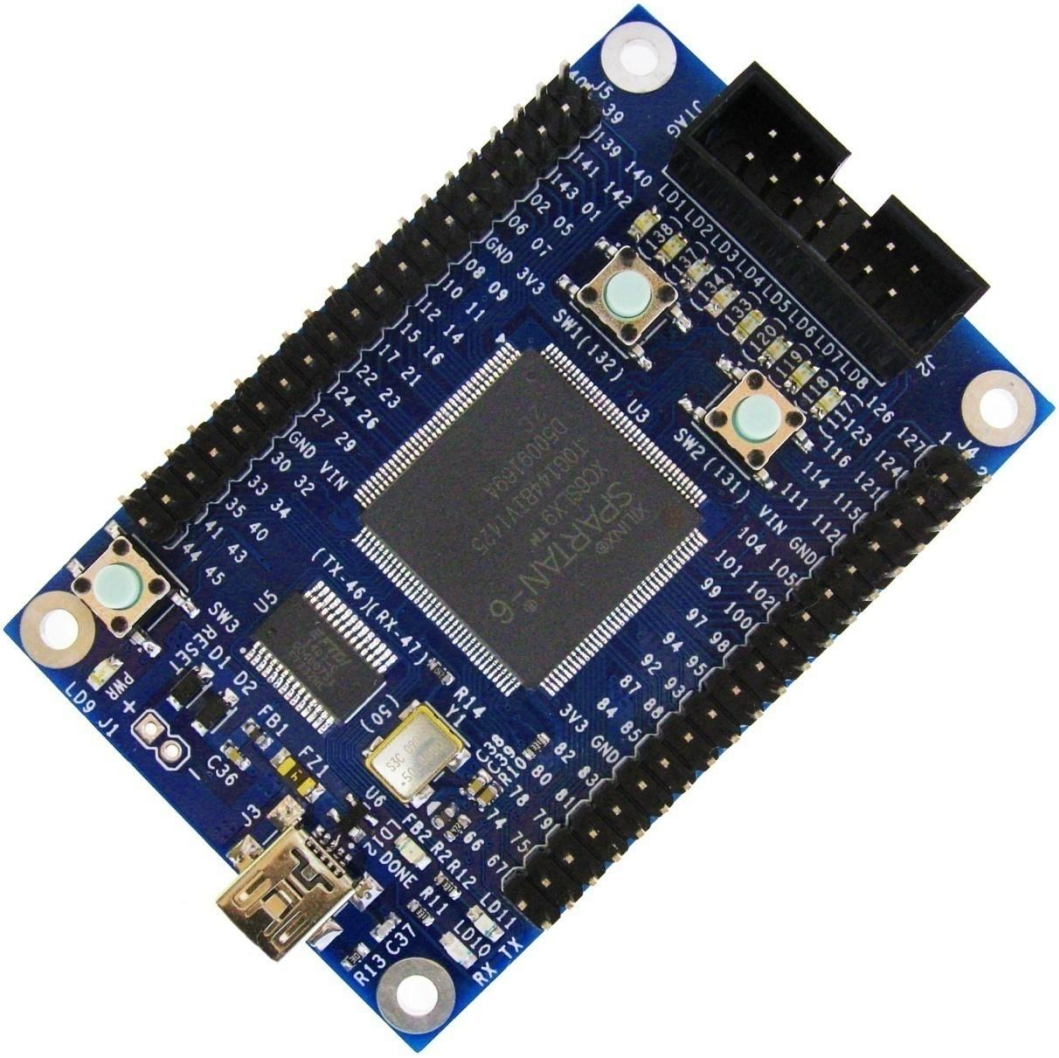
Xilinx XC6SLX9 Mini Board

User's Guide



1. Introduction

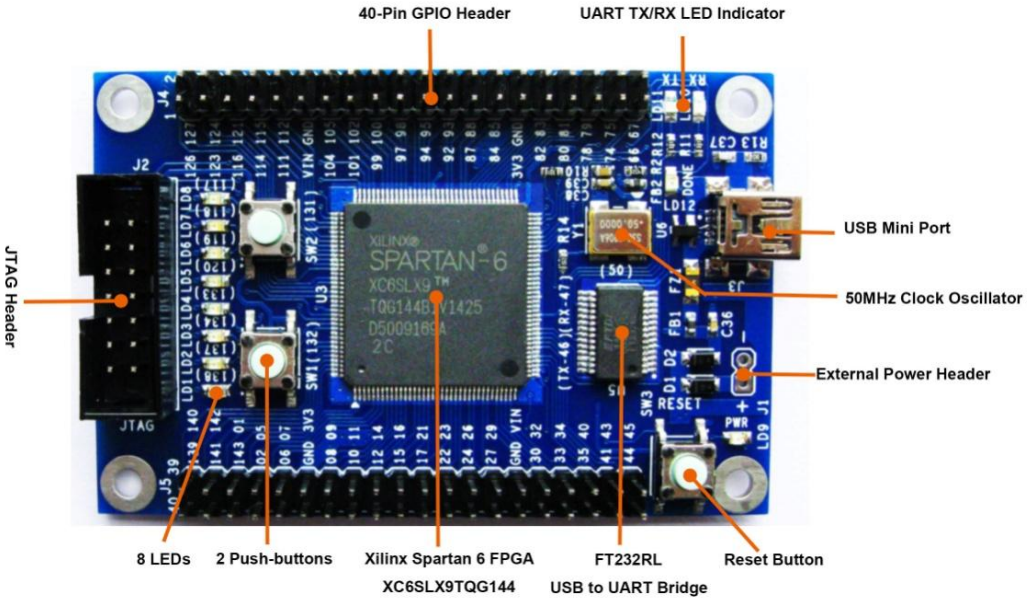
XC6SLX9 Mini Board is an easy-to-use FPGA platform based on Xilinx Spartan 6 series FPGA. It was initially designed for low cost with a everyone affordable price. Up to 72 I/O breakout makes it suitable in high pin count applications. You can connect the I/Os to your peripheral modules with several flying wires to quickly build a prototype project. Also, one USB to UART bridge is integrated on board, only a USB cable is needed for power supply and data communication. Because of its compact size and abundant IOs, it can be easily embedded in your design as a core. This guide describes how to use Xilinx tools and XC6SLX9 Mini Board to learn FPGA as a beginner. If you are familiar with Xilinx design tools and the process of FPGA design, some sections could be ignored.

The XC6SLX9 Mini Board includes:

– Xilinx Spartan 6 FPGA — XC6SLX9-2TQG144C(Spartan-6 FPGA Family Overview)
– 64-Mbit SPI Flash memory (W25Q64BV)
– USB to UART (FT232RL) with TXD, RXD activity LED Indicator
– Two groups of 2x20 expansion header (72 I/Os, +3.3V, +5V, GND)
– JTAG programming header, directly connected to Xilinx Platform Cable USB
– Two pushbuttons
– One reset pushbutton for reloading configuration file from external flash into FPGA
– Eight LEDs for I/O status indication
– 50 MHz clock oscillator
– USB or external power supply (can be powered with a 9V battery)

Board Size: 75(mm) x 49(mm)

XC6SLX9 Mini Board Layout (Top Side)



2. Get the tools ready

First, we must get the necessary software and hardware tools ready before starting a FPGA project. Three tools must be prepared:

1) **ISE WebPACK Design Software** — We use HDL(Hardware Description Language) code like Verilog or VHDL to describe a digital circuit, code must be compiled and ultimately implemented into a circuit layout that can be programmed to FPGA device. ISE WebPACK Design Software is an fully integrated tool for this purpose provided by Xilinx.
2) **XC6SLX9 Mini Board and one mini USB cable** — This board includes a target FPGA device and some other necessary circuitry and peripherals to support the running of the device.
3) **Xilinx Platform Cable USB or a parallel download cable** — This is a programming tool to download an configuration file generated by ISE WebPACK to the internal SRAM of the target FPGA device or an external non-volatile memory.

2.1 Download and Install ISE WebPACK Design Software

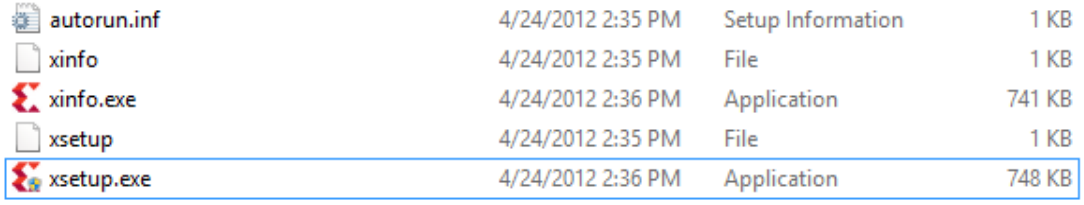
Xilinx provides a free IDE software named ISE WebPACK for beginners. Although it has limited functions compare to other charged editions, but that's enough for most beginners. It's a complete solution for FPGA design offering HDL synthesis and simulation, implementation, device fitting, and JTAG programming. Please visit ISE WebPACK Design Software webpage for details and download it to you PC. Different versions are provided, but they have similar UI and basic functions. Of course the latest version will occupy more hardware disk space. So which version you choose depends on your PC. **We use ISE WebPACK 14.1 for demonstration in this guide**.

Note: If you have installed ISE WebPACK Software on your PC, you can ignore this section.

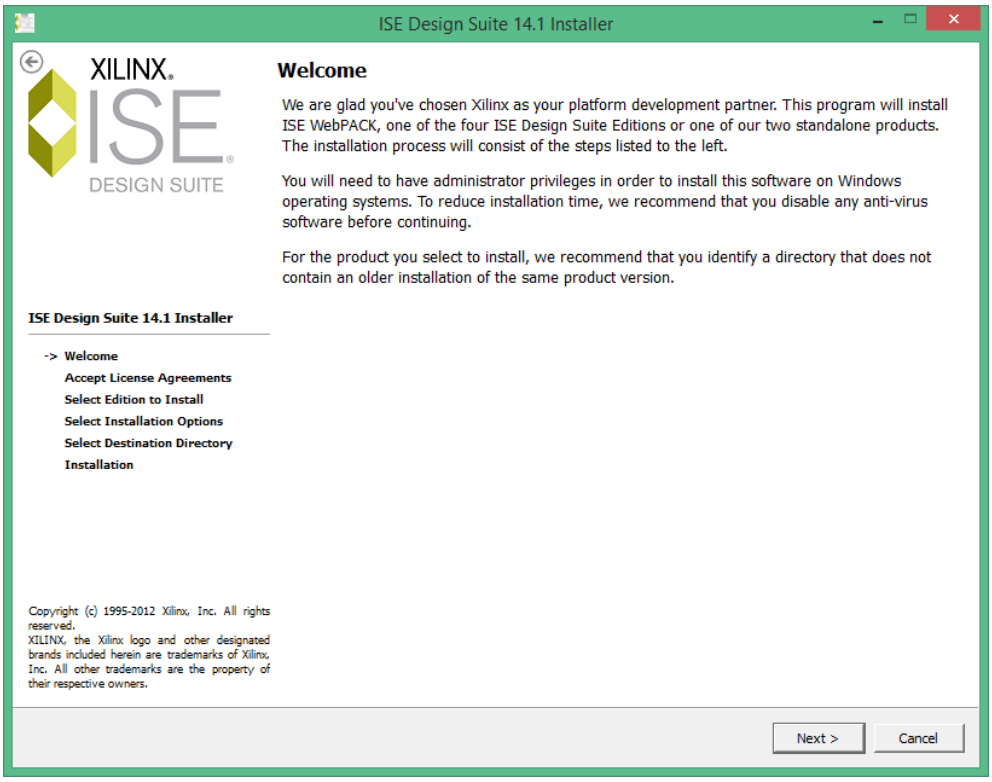
All the operations in the following sections are done on Windows 8.1 x64 operating system.

2.2 Install the ISE WebPACK Design Software

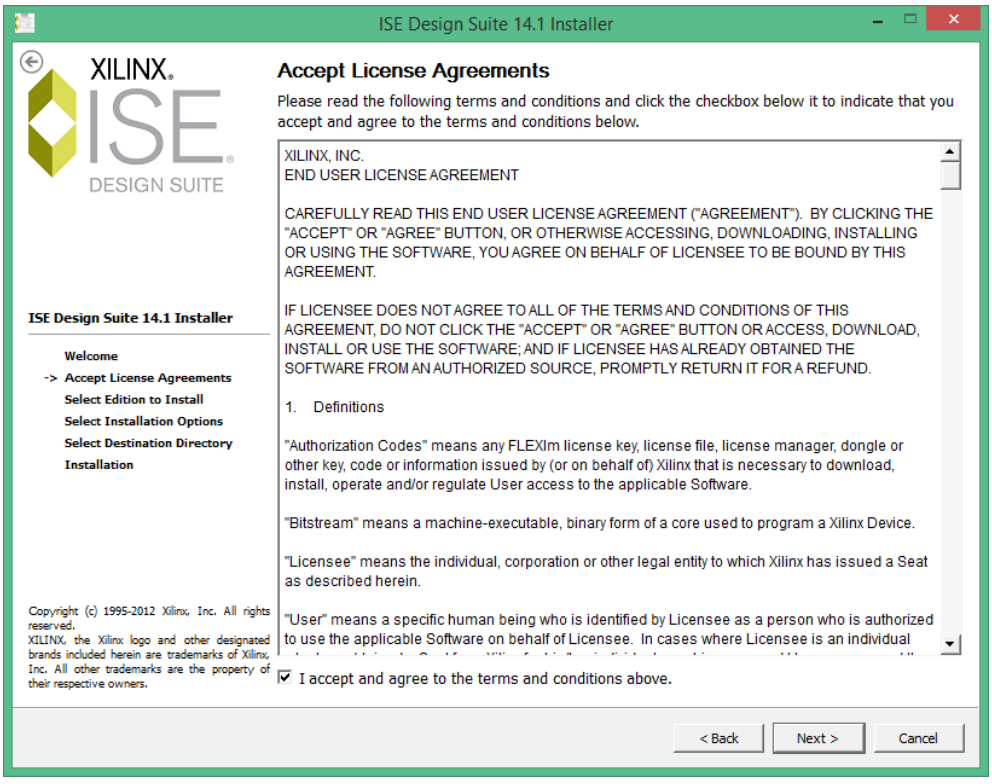
1) Unzip the download file and go to the setup directory, double-click **xsetup.exe** to start the installation process.



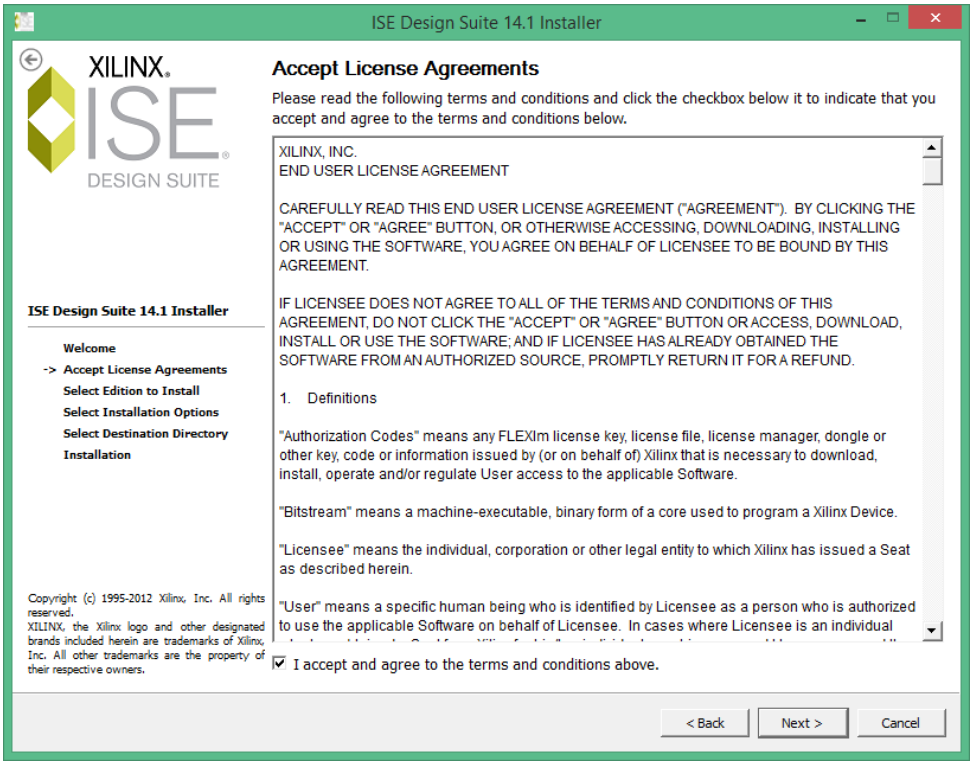
2) A welcome window appears, click **Next** to next window.



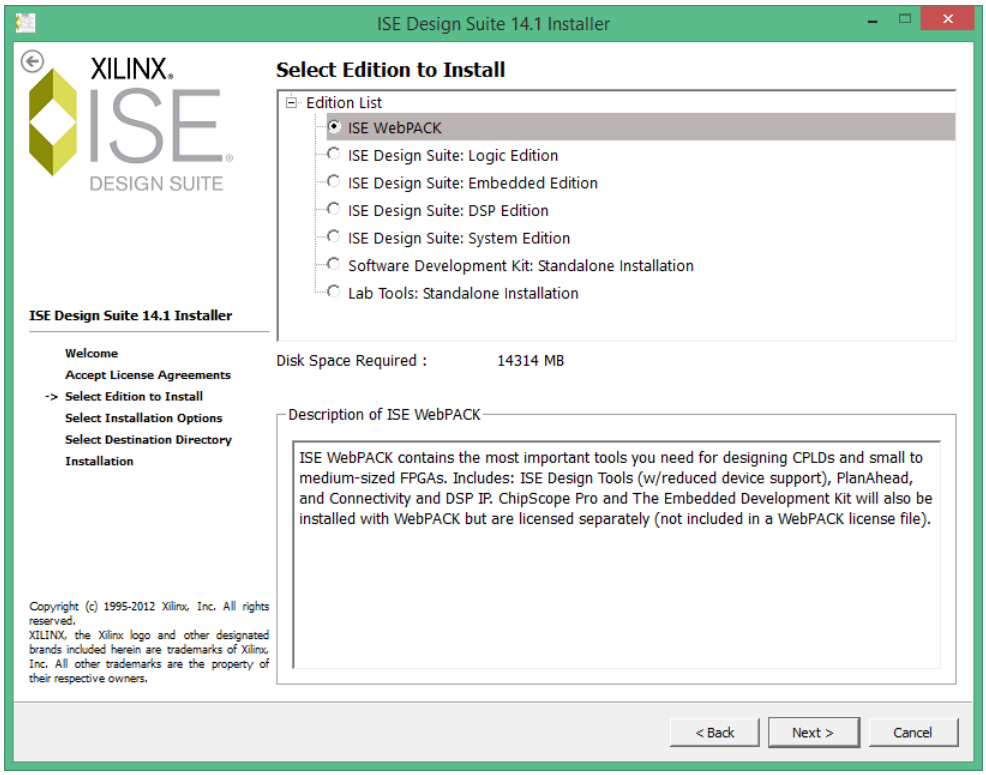
3) Enable the checkbox to accept terms and conditions, click **Next** to next window.



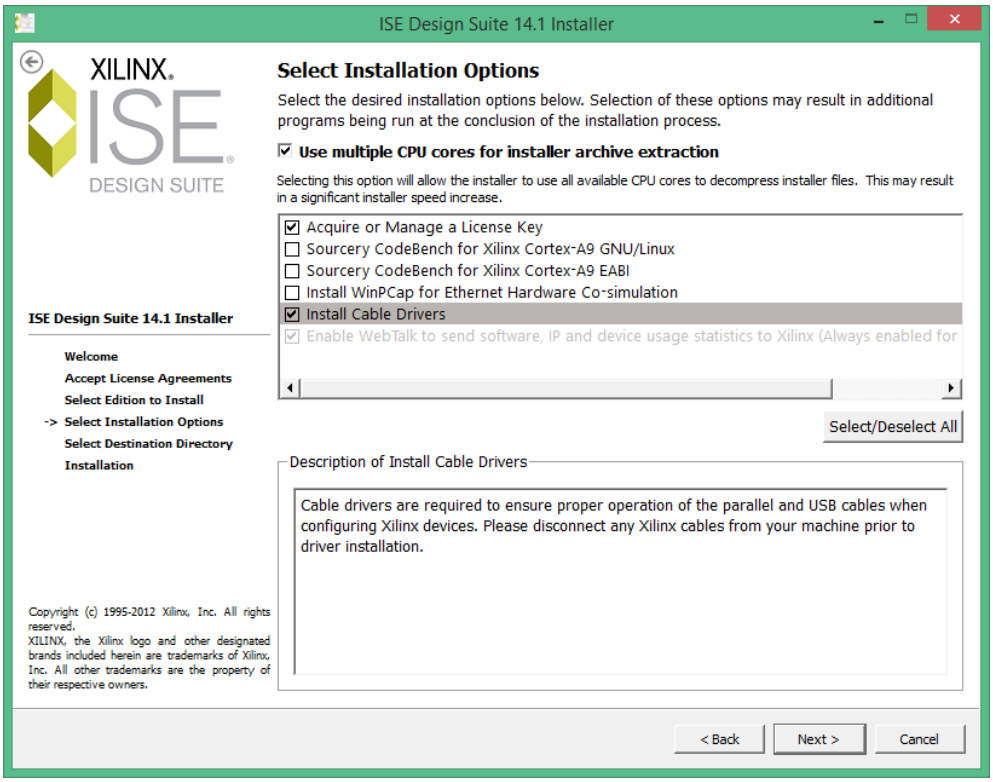
4) Another license agreement window appears, enable the check box, and click **Next** to next window.



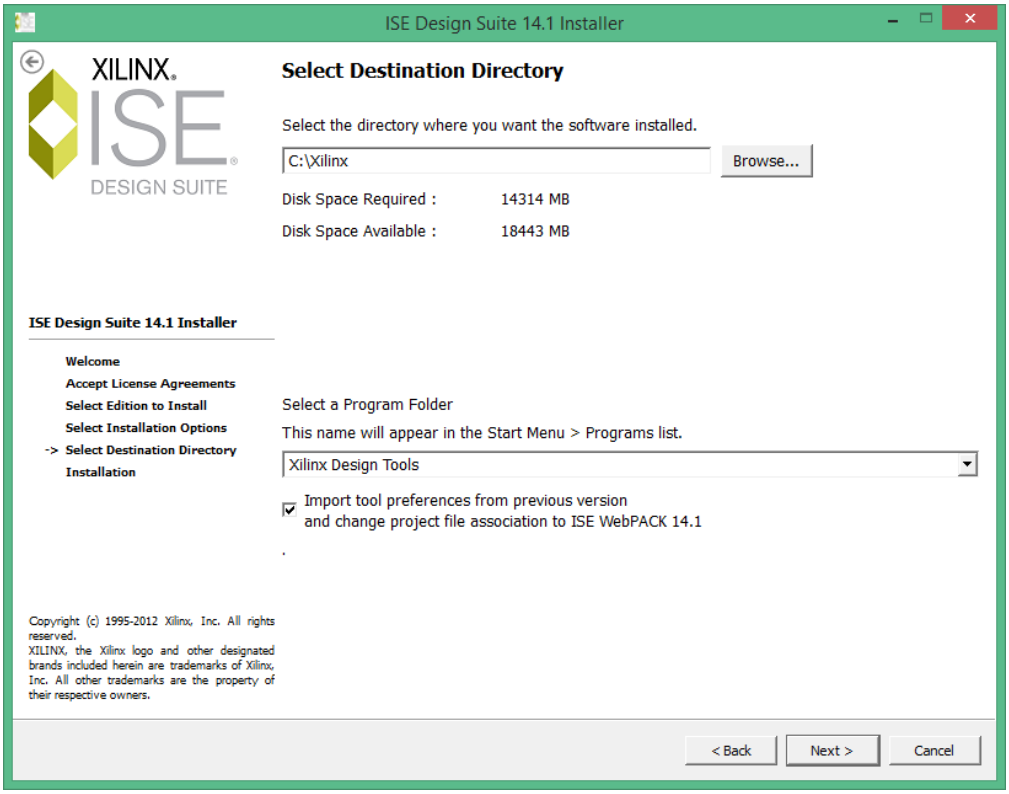
5) Different editions are contained in this ISE Design Suite. We select ISE WebPACK. Click **Next** to next window.



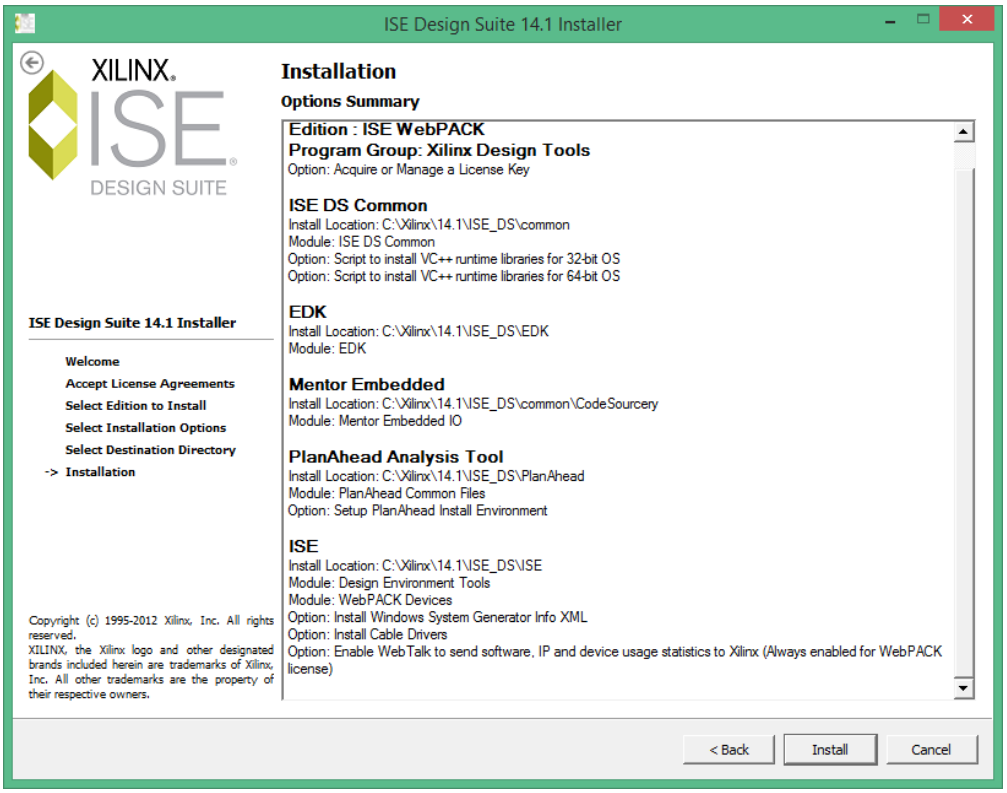
6) Select the options as shown below. Click **Next** to next window.



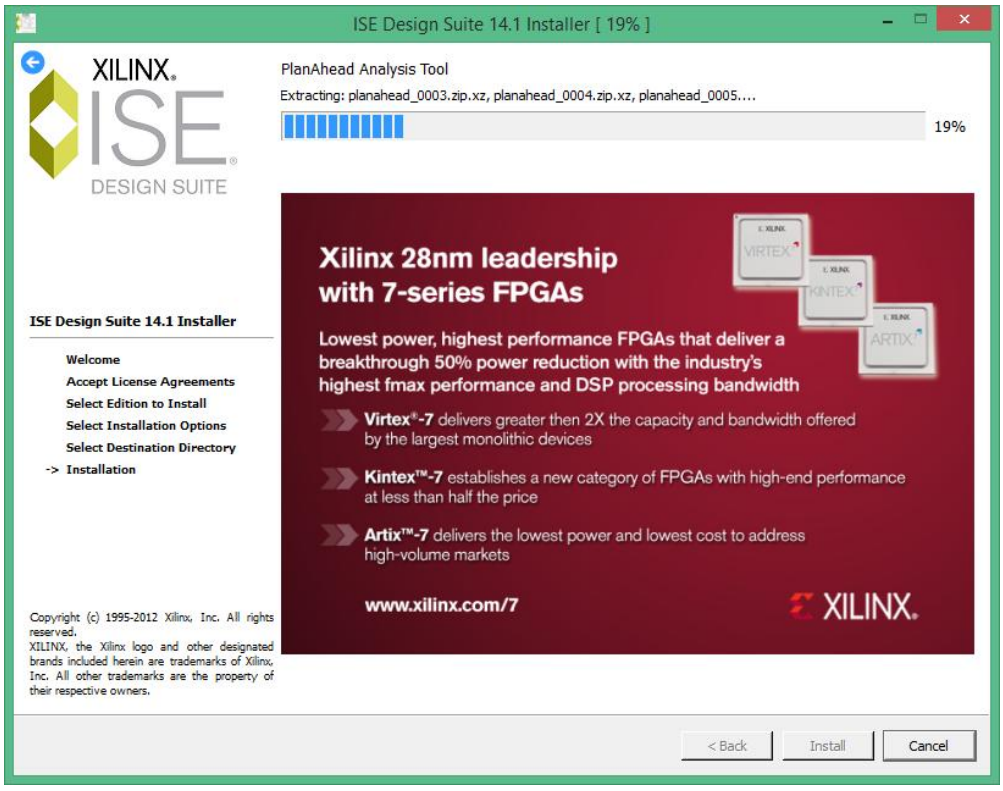
7) Select destination directory. You can change to other directory if you don't have enough space in C disk. Click **Next** to next window.



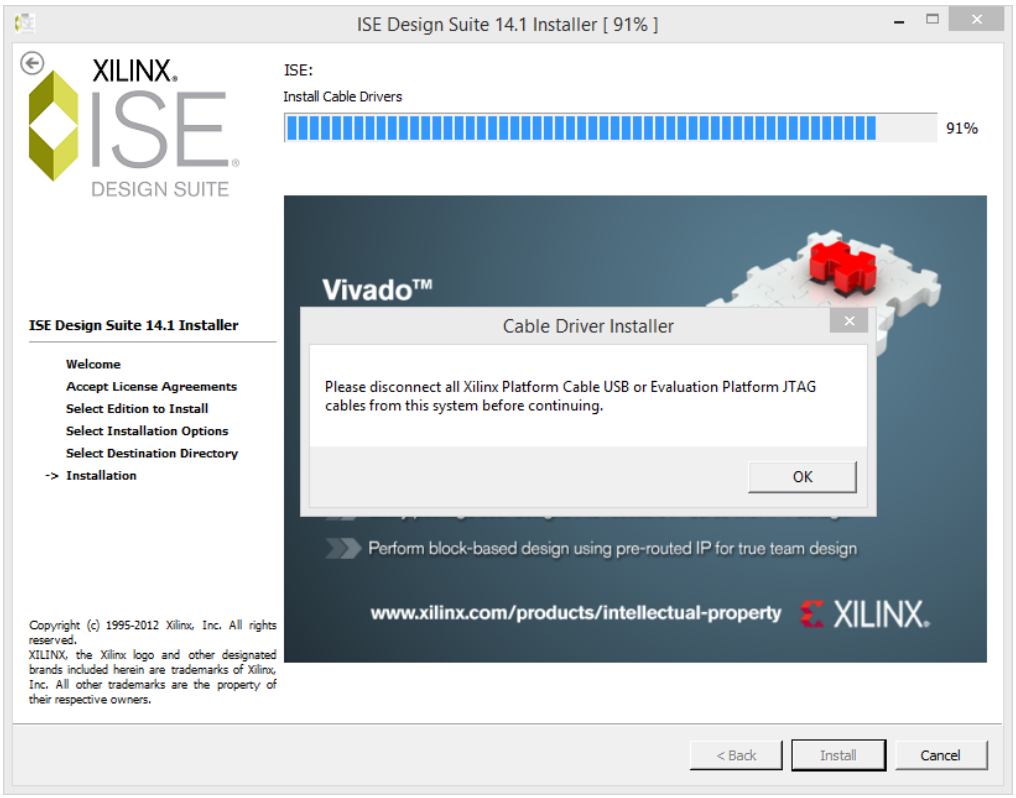
8) A summary window lists the tools and components that will be installed, click **Install** to start the installation.



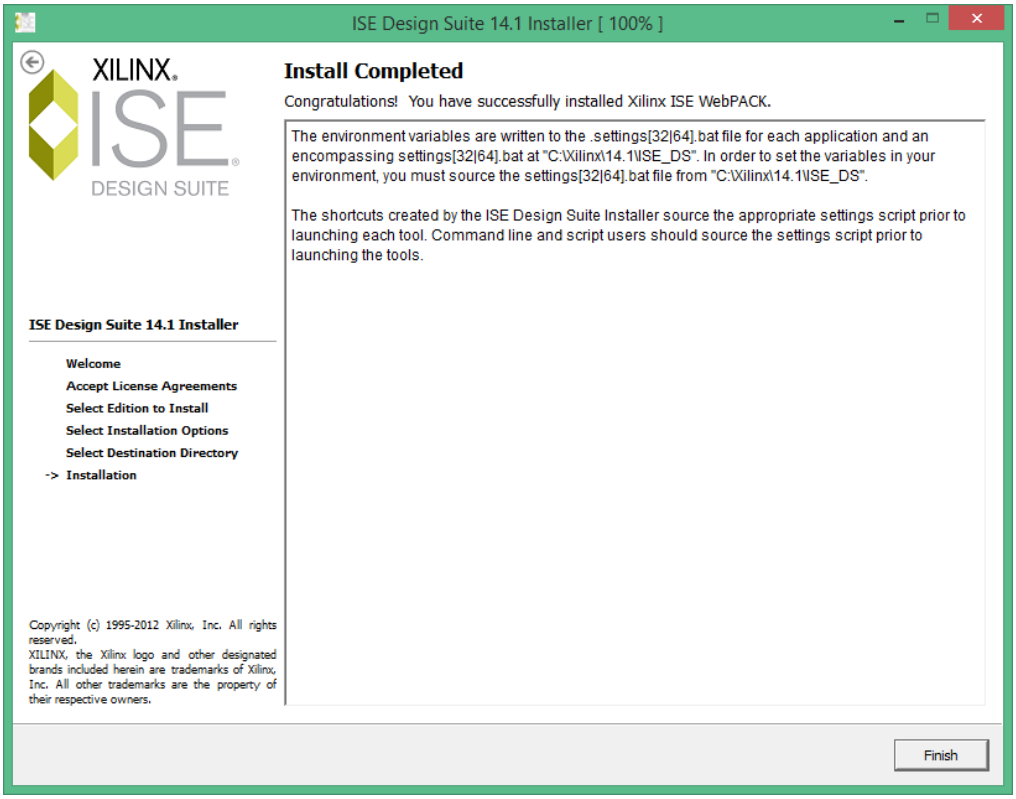
9) It may take several minutes to complete the installation, please wait patiently.



10) A message box may pop up to inform you to disconnect all Xilinx Platform cables. Remove the cables and Click **OK**.

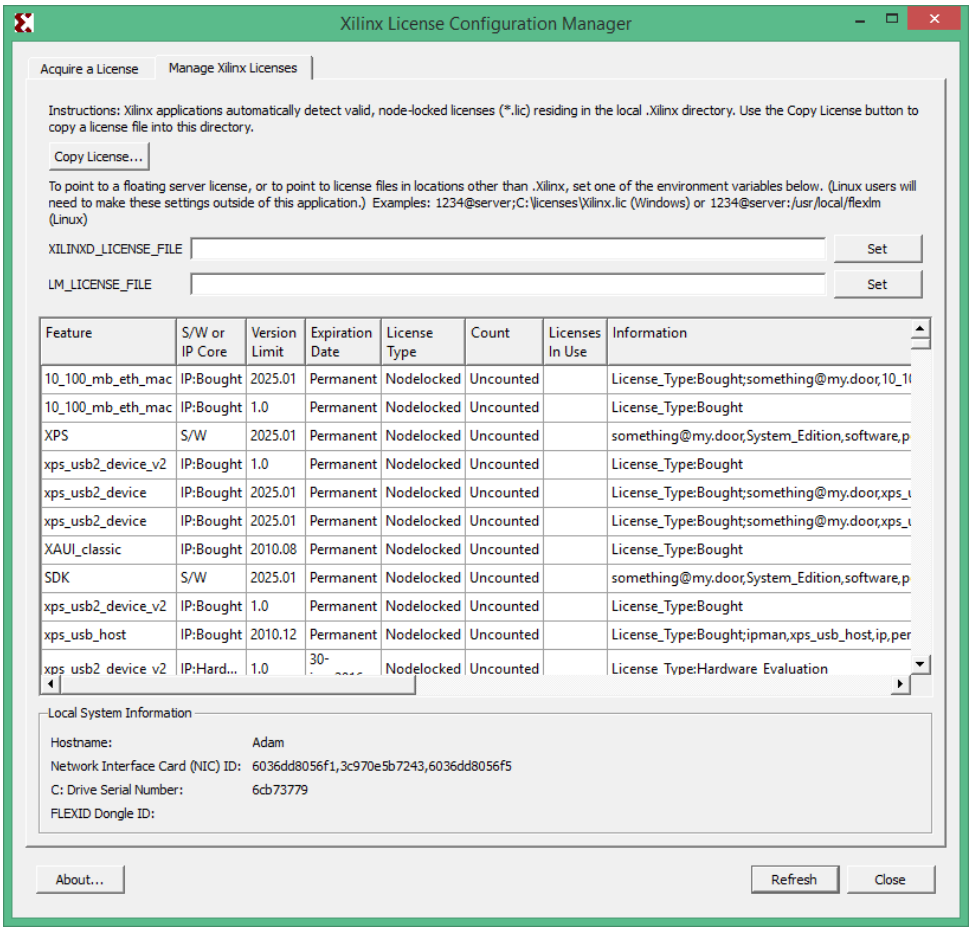


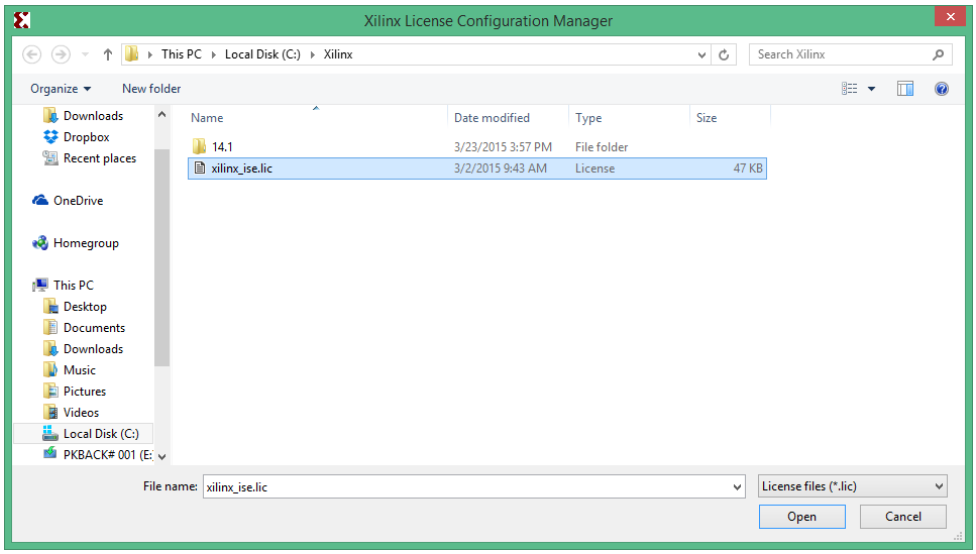
11) Click **Finish** to complete the the installation.



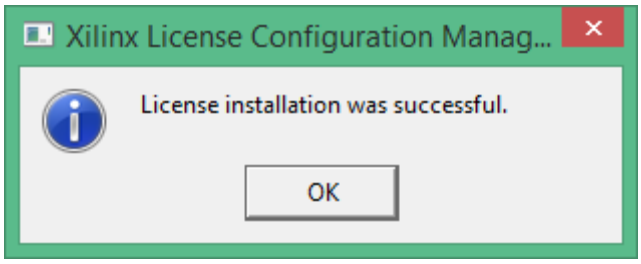
12) To Get a free license from Xilinx, you must register a user account on Xilinx Website and apply for a free license for ISE WebPACK. The details are ommited here, just follow the instructions on the website, you will get the license file easily.

13) After receiving a license from Xilinx, copy the license file to the destination directory where the software is installed. Enter **Manage Xilinx License**s tab, click **Copy License...** , and then locate the license file with **.lic** suffix.





14) Congratulations! You have successfully installed and activated the software.



2.3 Setup the XC6SLX9 Mini Board

A USB connection is provided on XC6SLX9 Mini Board. It is intended for data communication and powering the board. FT232R is used as a USB to UART bridge. It is a very popular IC widely used in various USB converter cables. As usual, a device driver software must be installed before the operating system could successfully recognize and operate the device.

Note:

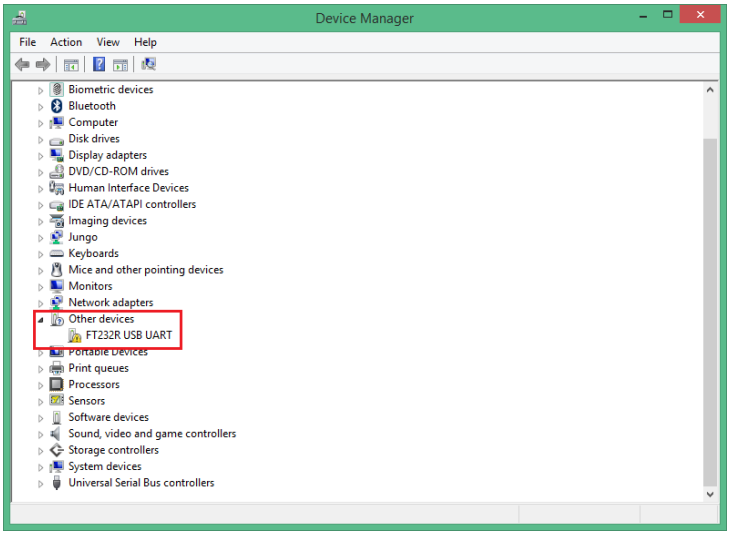
1) If your PC has the driver software installed before, the on-board FT232R will be enumerated as a common serial port when you connect the board to PC.

2) For the latest operating system like Windows 8, when a USB device detected, it will automatically find and install the driver for the device if windows update is enabled and internet connection is available.

The following instructions describe how to install the driver software for FT232R:

1) Power the board

Plug the XC6SLX9 mini board to your PC via a USB mini cable. When powered, the windows system will detect the insertion of a USB device and try to load a driver for this device. If windows fail to find the driver, it will list the device in the Device manager with a yellow exclamation mark, indicating the driver for this device is not found.



2) Install driver software automatically(Internet connection must be available)

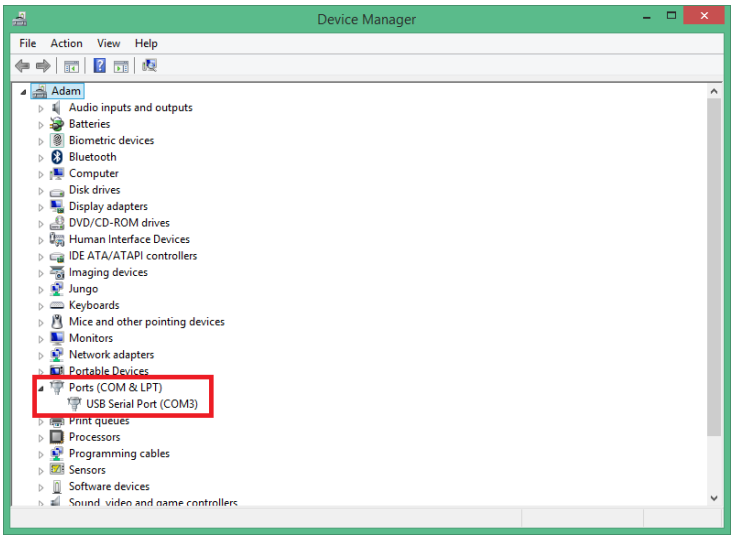
- Right click on the FT232R USB UART, and select **Update Driver Software...**
- Select **Search automatically for updated driver software**
- Windows will automatically find and install the driver software, this will take a few seconds.

3) Install driver software manually

- Download the driver software from FTDI website according to the edition of your operating system.
- Now, for Windows system, an executable version of this driver is available, unzip and run the executable file, driver will be installed automatically.

4) Verify the result

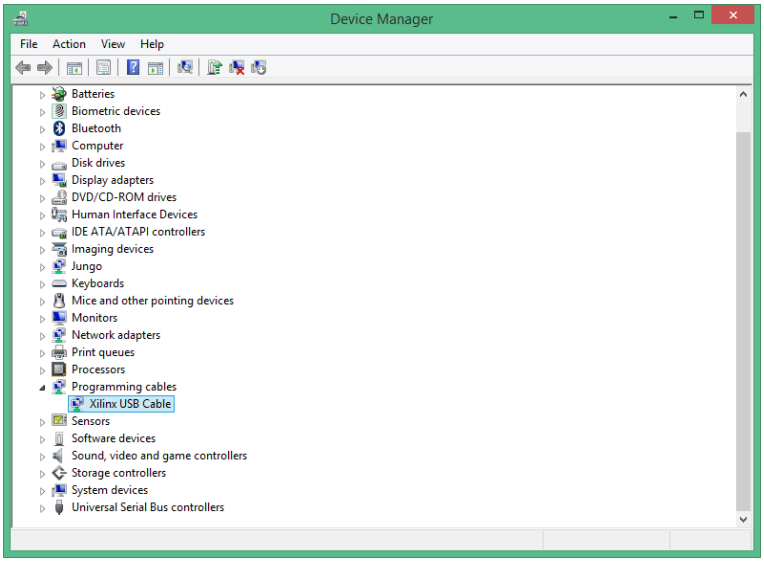
If the driver software is properly installed, the FT232R will function as a virtual serial port. And it will appear in the Device Manager list.

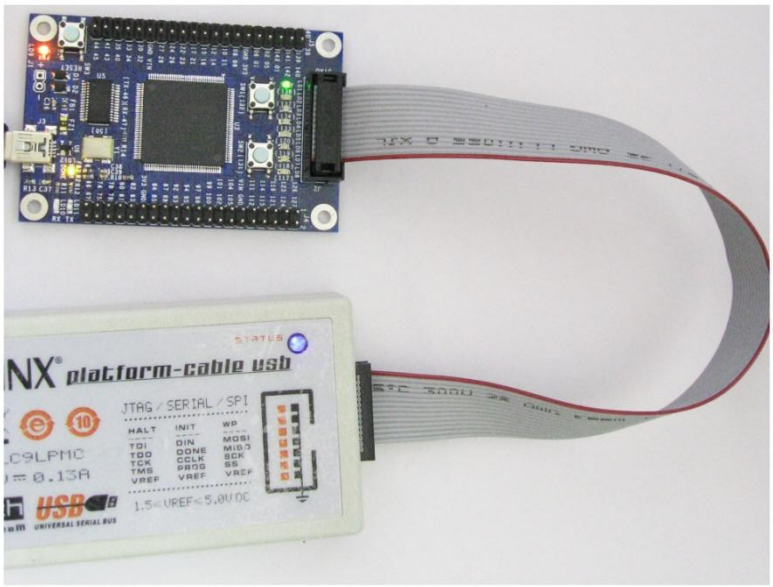


Note: You must get a serial port monitor software like PuTTY to hunt the serial port activities.

2.4 Setup Xilinx Platform Cable

A download cable is needed to program the configuration file to the target FPGA device. Xilinx provides USB download cable and parallel download cable, but USB cable is more popular because parallel port is eliminated in most new generation desktop or laptop PCs. We use Xilinx Platform Cable USB in all the demos and examples. A USB driver software is needed for this cable. It's integrated in the ISE WebPACK Design Software and has been installed in previous installation process. If the driver doesn't work or crashed, please read the application guide USB Cable Installation Guide, and reinstall it. If driver software is properly installed, the cable named **Xilinx USB Cable** will appear in the Device Manager list.



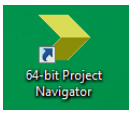


3. Create your first FPGA Project

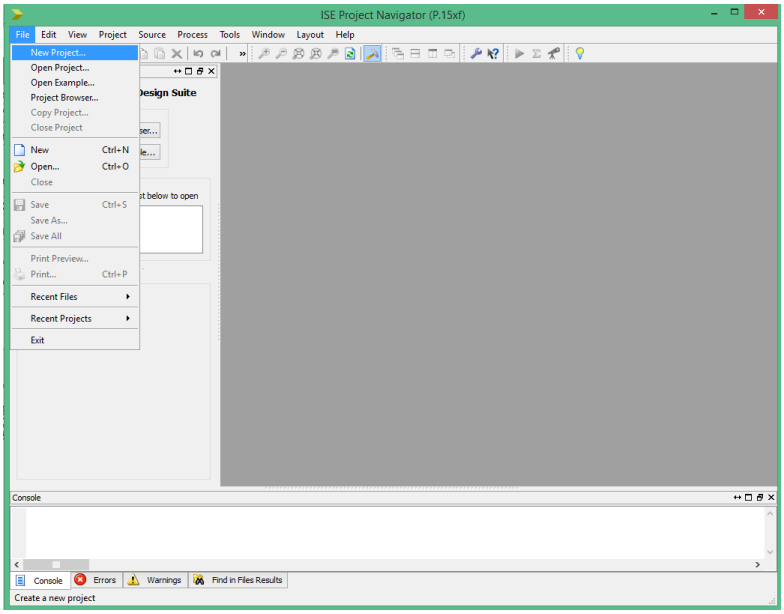
This section will guide you through the process of creating a simple FPGA project using Verilog HDL. We build an 8-bit barrel shifter that rotates one bit to the right in the interval of 1/4 second. The state of the shifter will be displayed on the eight LEDs. And finally, the object file will be downloaded to the target device on XC6SLX9 Mini Board and got verified.

Note: Some procedures like simulation, timing analysis, and creating constraints in FPGA design are omitted in this section.

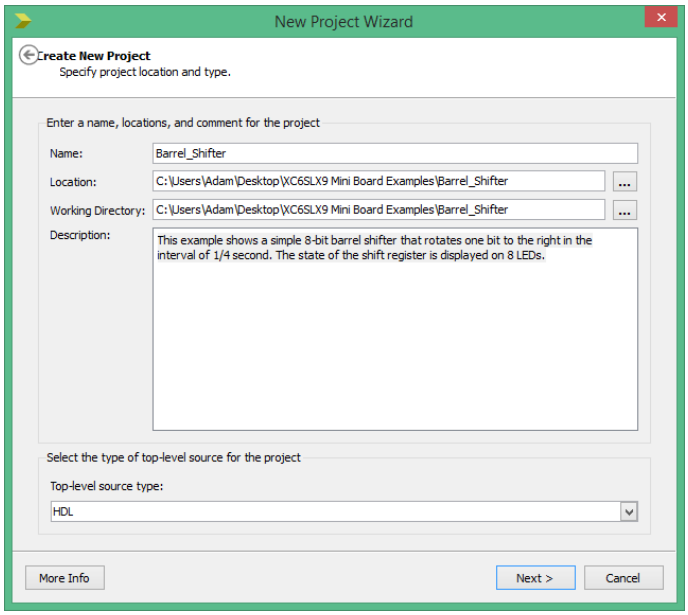
1) Double-click **ISE Project Navigator** icon to start the IDE.



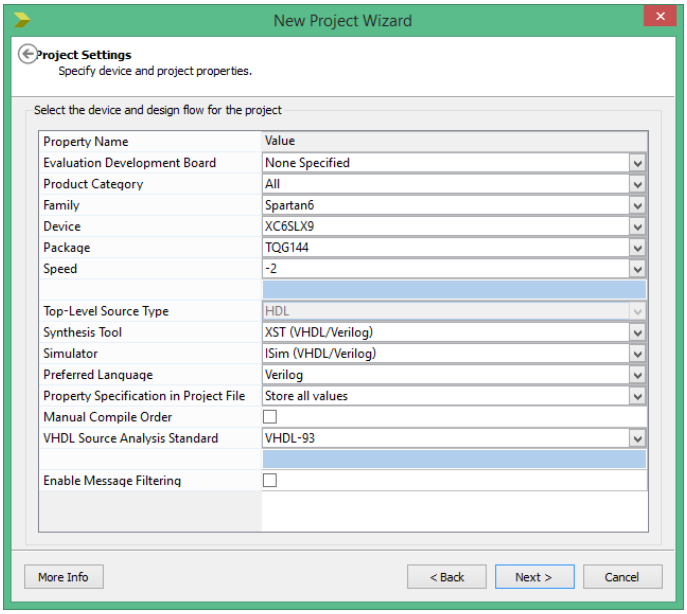
2) Select **File -> New Project...** The New Project Wizard appears.



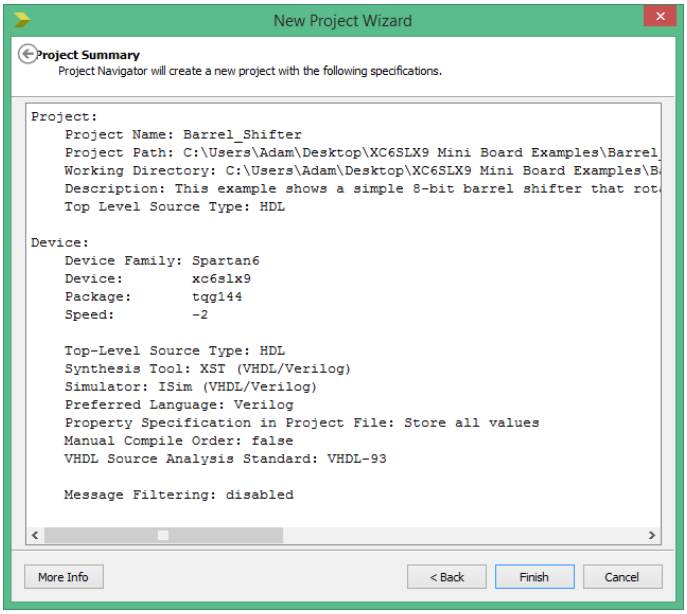
3) Type **Barrel_Shifter** in the Project Name field. Browse to a location (directory path) for the new project. A Barrel_Shifter subdirectory will be created automatically. Select HDL in the **Top-Level Source Type** list. Click Next to move to the device property window.



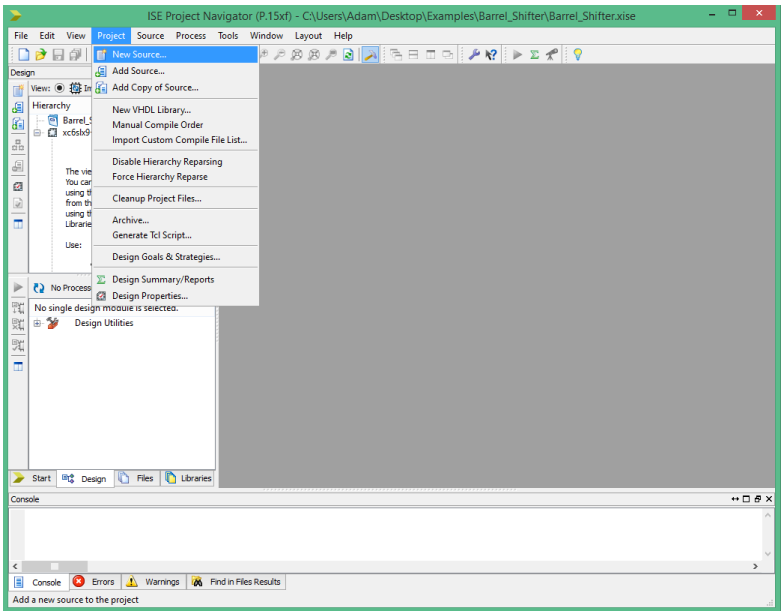
4) Select a value for Device, Package, Speed and other properties as shown below.



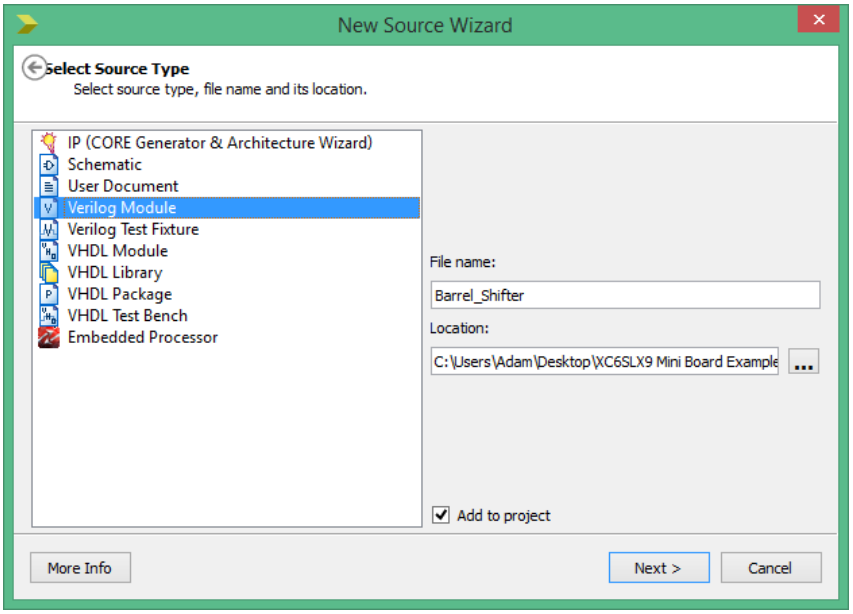
5) A summary window appers.Click finish to comlete the project wizard.



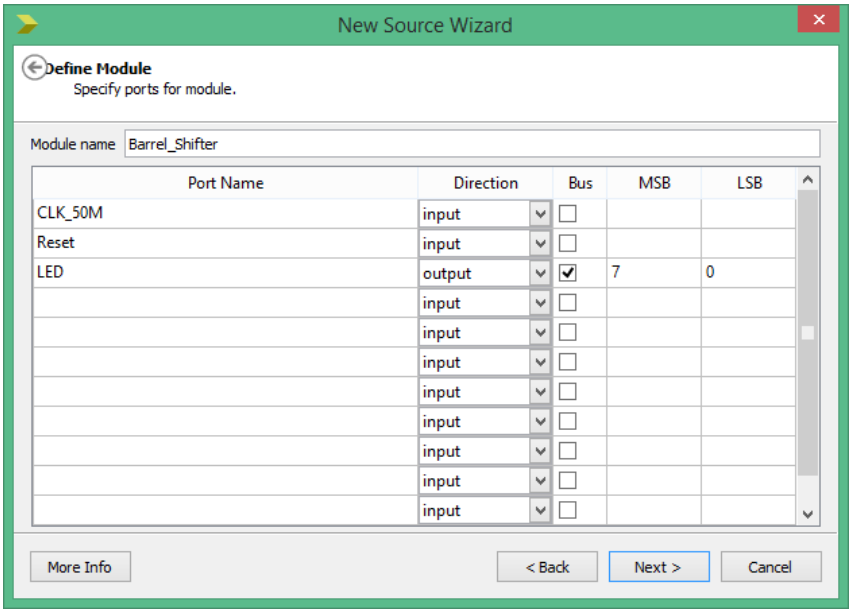
6) Click **Project -> New Sources...** to create an HDL source.



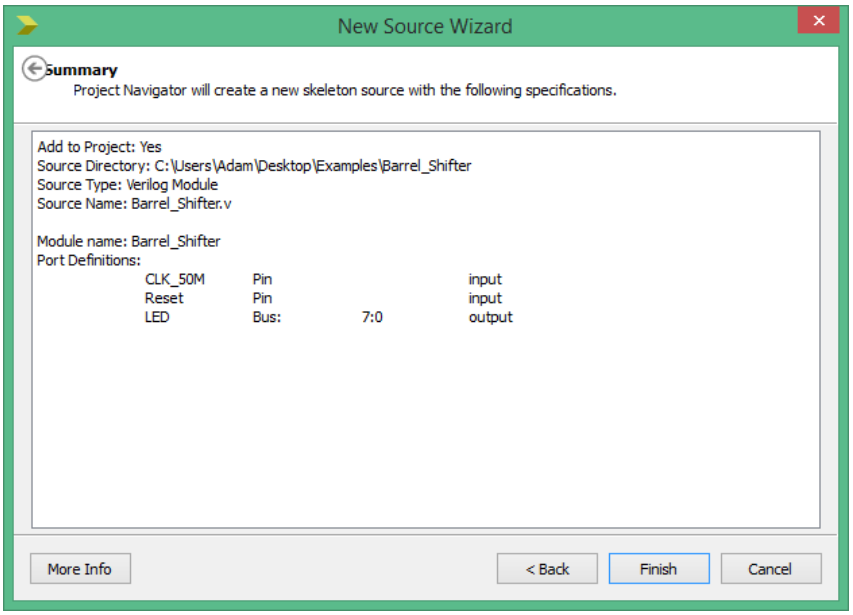
7) Select **Verilog Module**, enter the file name **Barrel_Shifter**. Leave the file location to the default. Verify that the **Add to project** checkbox is selected. Click **Next** to next window.



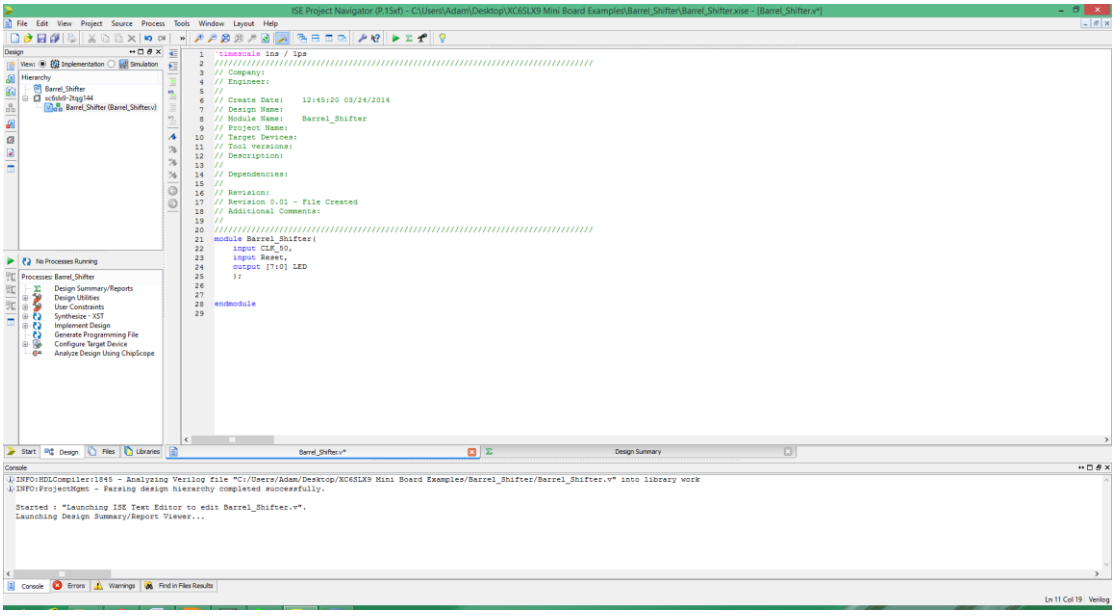
8) Declare the input and output ports for the module as shown below,and then click Next to next window.



9) A summary window displays the information you entered in previous steps. Click **Finish** to complete the wizard if no errors found.



10) The module head and some comments about this module have been added to the source code file automatically.

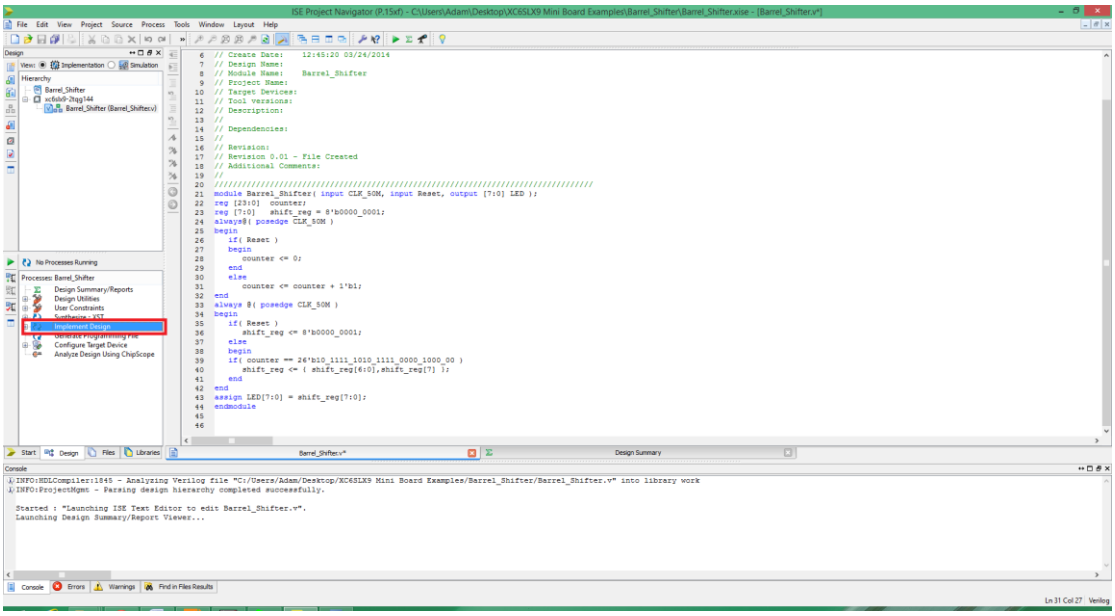


11) Copy the HDL code shown below to the Barrel_Shifter source file and save the file.

Note: If you are new to Verilog HDL and can't understand the meaning of the code, please don't worry about that. You will get familiar with the coding rules after reading a Verilog HDL book. We mainly focus on learning the tools of Xilinx FPGA, not the details of Verilog HDL in this guide.

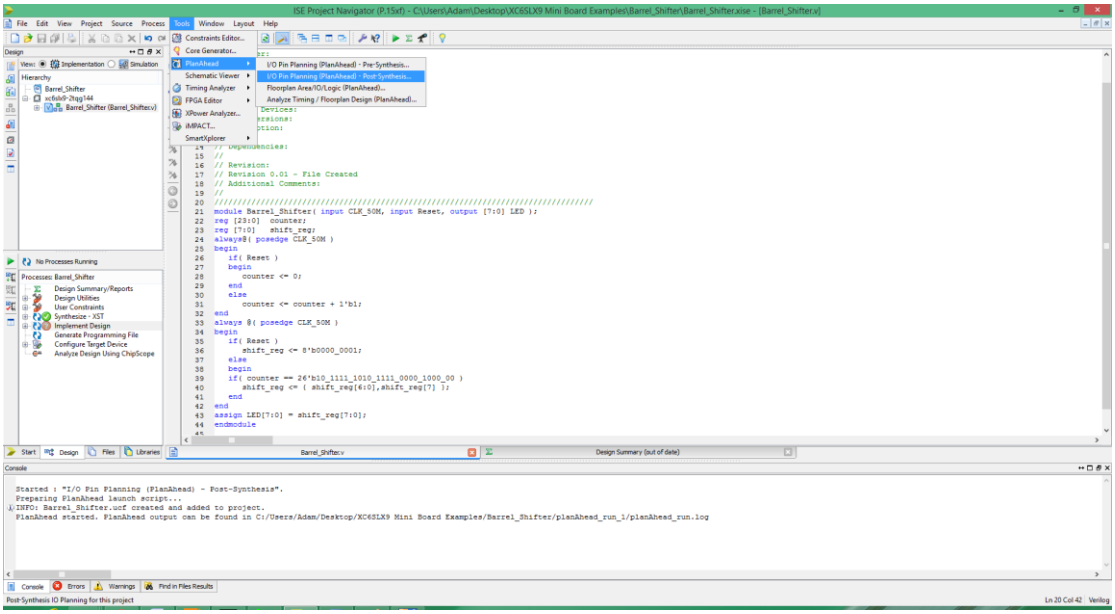
```
module Barrel_Shifter( input CLK_50M, input Reset, output [7:0] LED );
reg [23:0]    counter;
reg [7:0]     shift_reg = 8'b0000_0001;
always@( posedge CLK_50M )
begin
   if( Reset )
   begin
        counter <= 0;
   end
   else
        counter <= counter + 1'b1;
end
always @( posedge CLK_50M )
begin
   if( Reset )
        shift_reg <= 8'b0000_0001;
   else
   begin
   if( counter == 24'b1011_1110_1011_1100_0010_0000 )
        shift_reg <= { shift_reg[6:0],shift_reg[7] };
   end
end
assign LED[7:0] = shift_reg[7:0];
endmodule
```

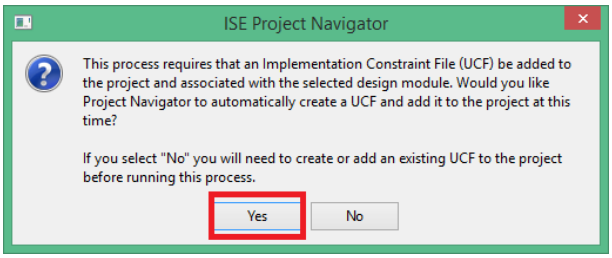
12) Double-click **Implement Design** in the process window. The project will be parsed and synthesized successfully.



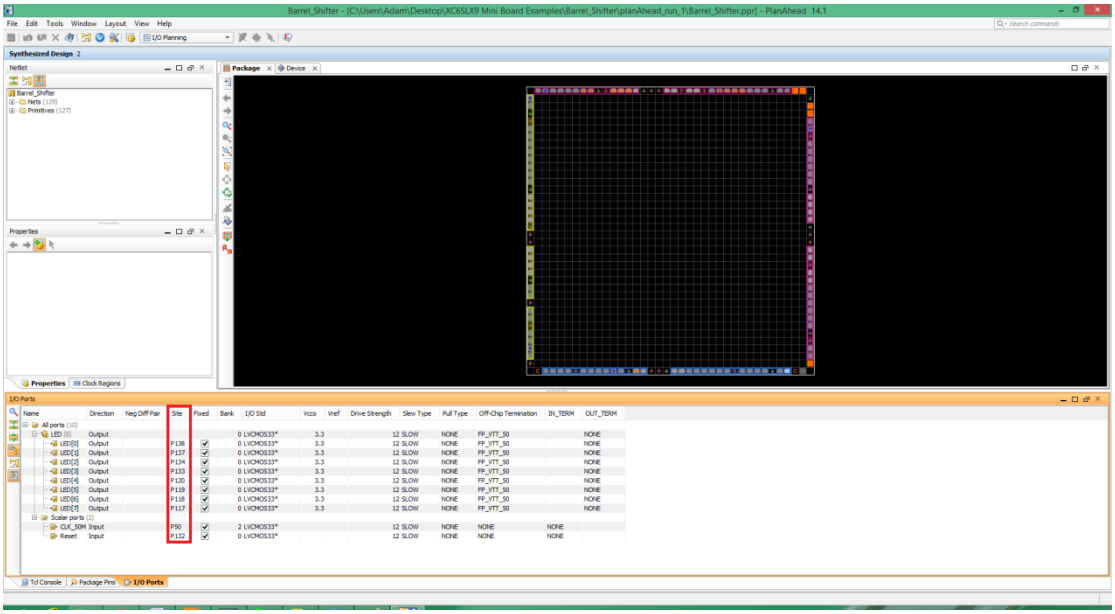
Note: Since the source code is verified, you don't need to correct any syntax errors or typos. In most cases, error is unavoidable for beginners, you should learn to analyze the error or warning tips printed in the Errors and Warnings window.

13) Click **Tools** -> **PlanAhead** -> **I/O Pin Planning(PlanAhead)-Post-Synthesis...** to assign pin locations. Then click **Yes** to automatically create a new constraint file add it to project.



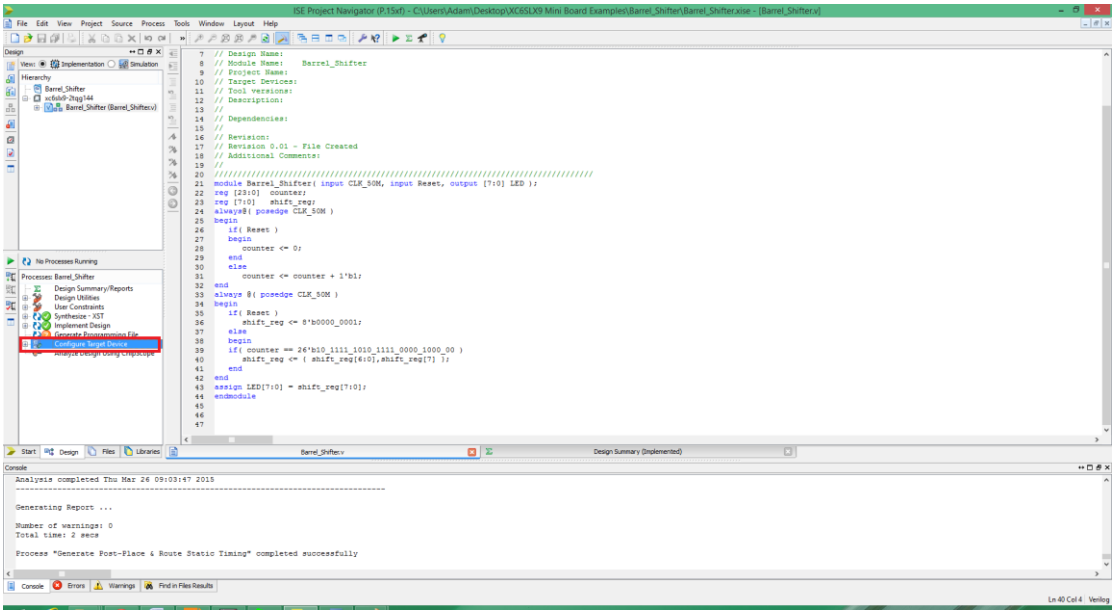


14) Assign pin locations as shown below and then save the constraint.



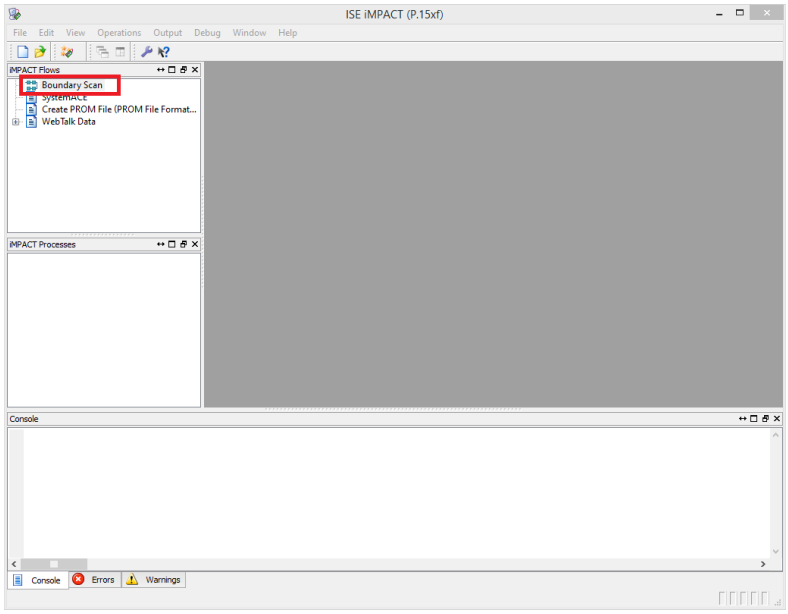
15) Reimplement the design.

16) In the Process window, double-click the **Configure Target Device** process. The system will automatically generate an configuration file for programming, and then iMPACT software will be launched.

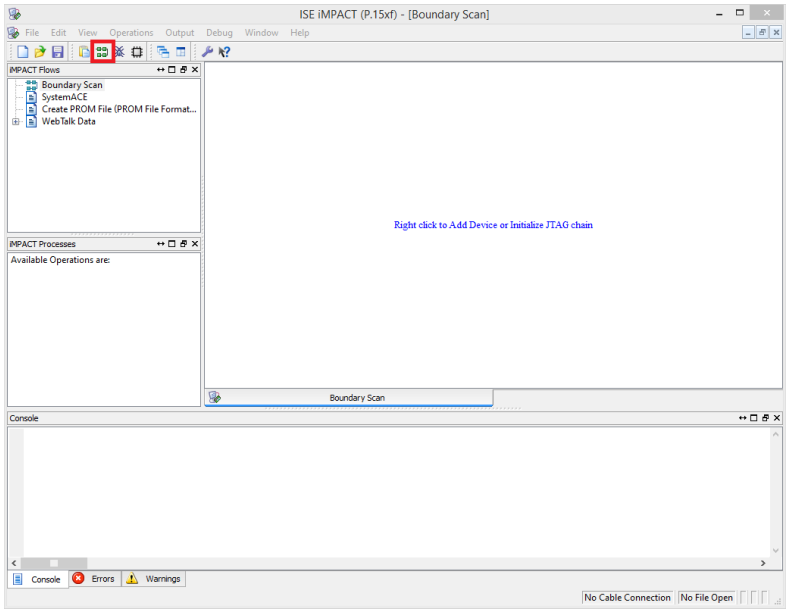


17) In the ISE iMPACT window, double-click **Boundary Scan**.

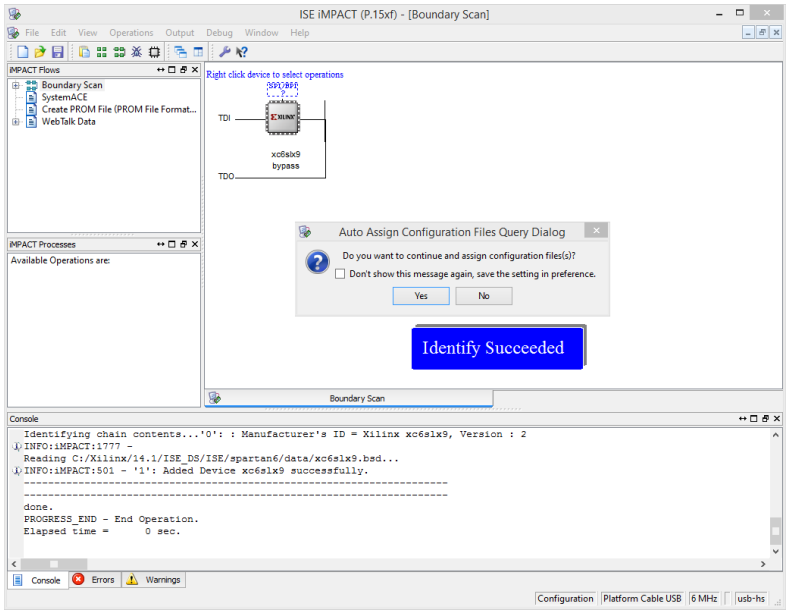
Note: To successfully find a device in the JTAG chain, Xilinx Platform cable USB must be connected to the XC6SLX9 Mini Board, and both should be powered.



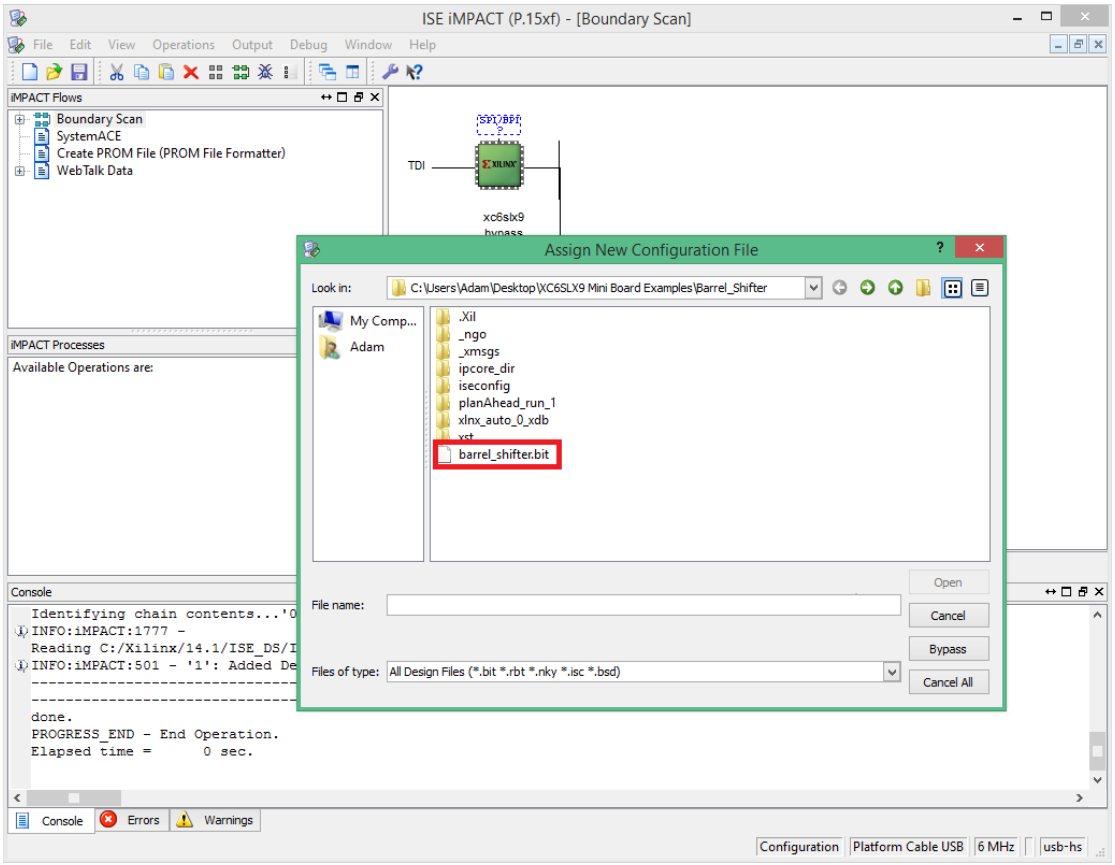
18) Click the **Initialize Chain** command, iMPACT will automatically search devices available in the JTAG chain and display the result in the **Boundary Scan** window.



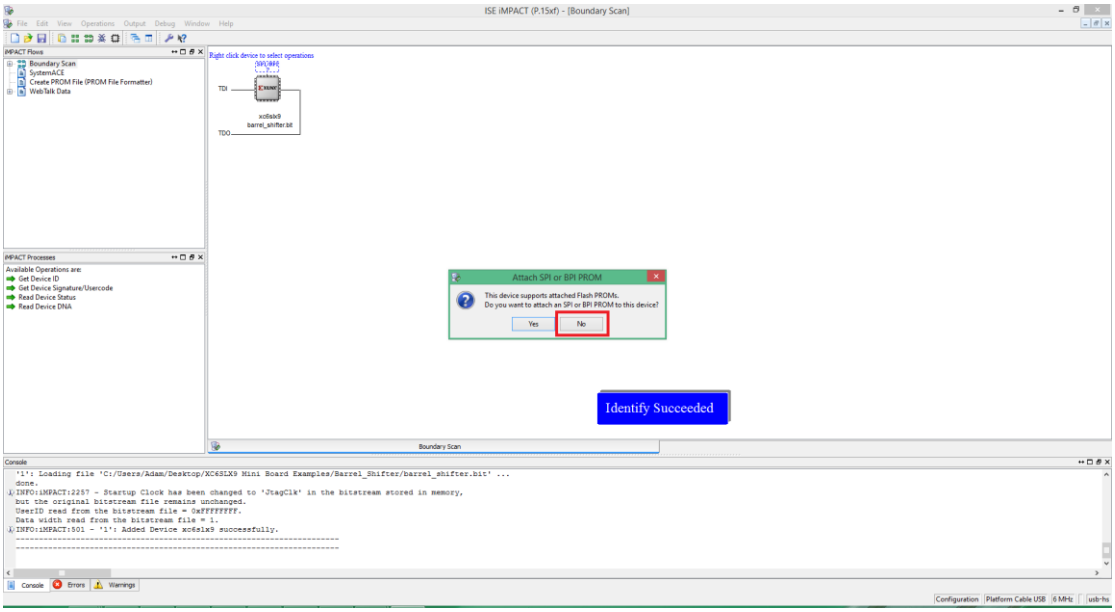
19) When a device detected, click **Yes** to assign a configuration file.



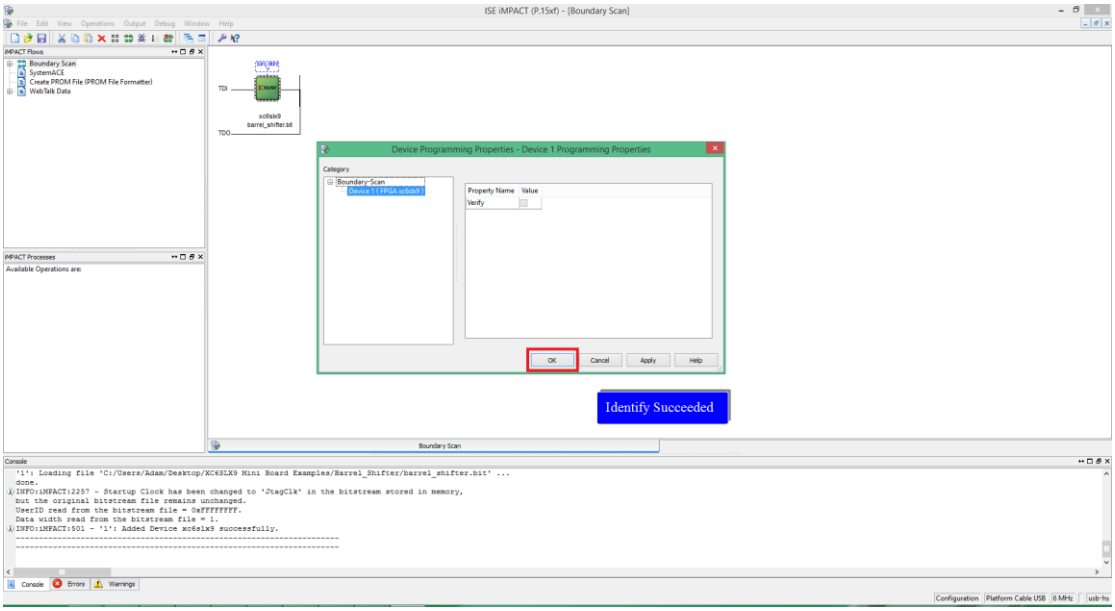
20) The generated configuration file is saved under the project directory. Locate the file and click **Open** to load it into the iMPACT software.



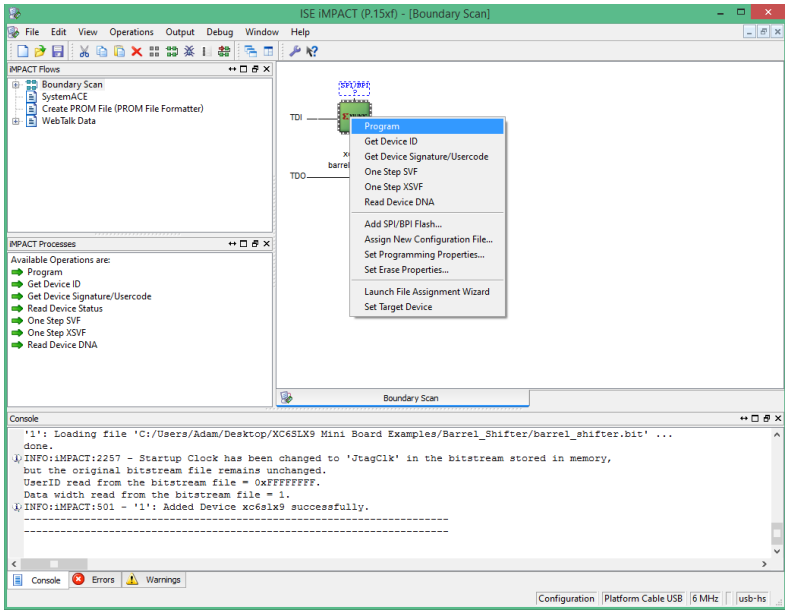
21) When a message box appears and ask if you want to attach a SPI or BPI PROM. Click **No**. We will program the SPI flash later.



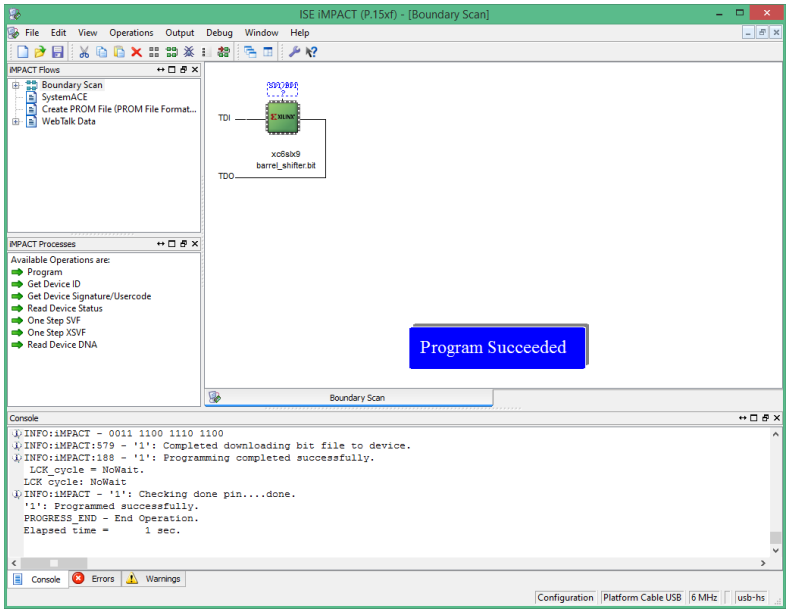
22) A Device Programming Properties window may pop up. Click **OK**.



23) Right-click the  icon and select **Program** command. iMPACT will initiate the download process.

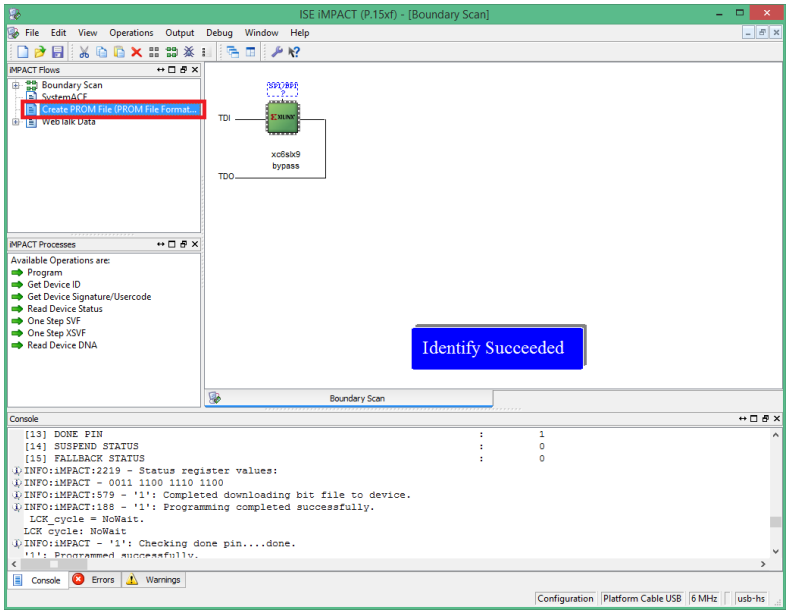


24) When programming is complete, the Program Succeeded message is displayed. Now, you can find only one LED is lit on board and rotating from left to right.

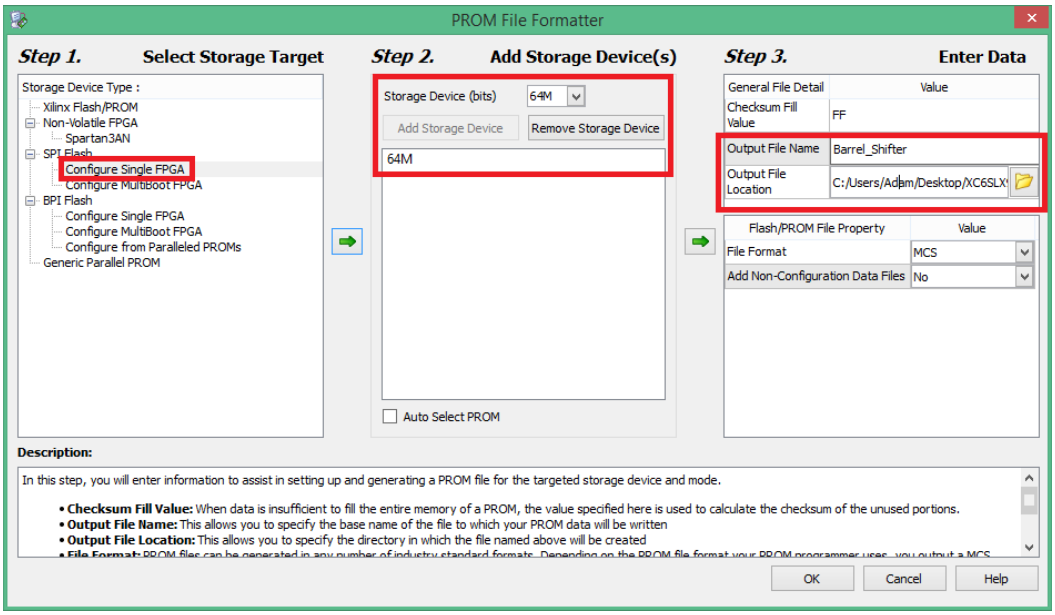


Note: In the previous steps, the configuration file is downloaded to the SRAM of the target device. As we know, SRAM is a kind of volatile memory, that means data stored in SRAM will be lost when power is removed. The XC6SLX9 Mini Board has a non-volatile SPI flash(W25Q64BV) to store the configuration file. Data will be automatically loaded into the SRAM of FPGA device during power up. The following steps will show you how to generate a PROM file and program it to the SPI flash.

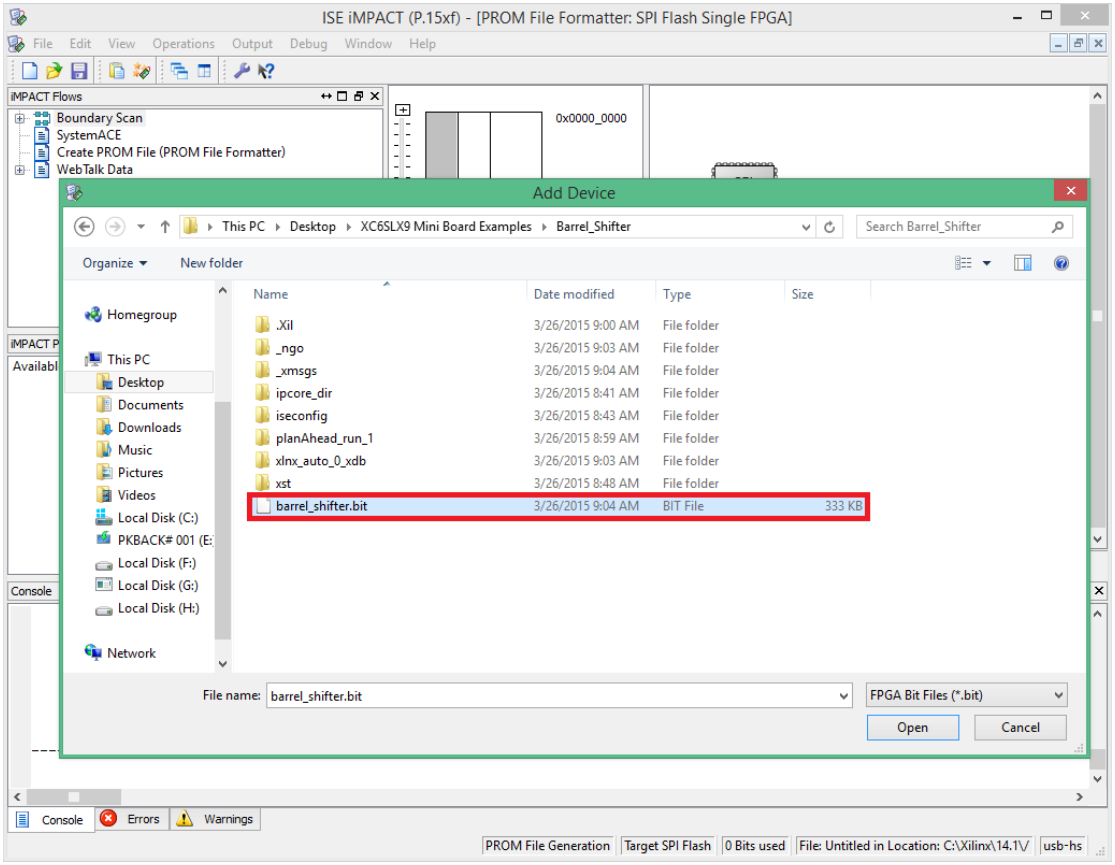
25) Double-click **Create PROM File(PROM File Formatter)**.



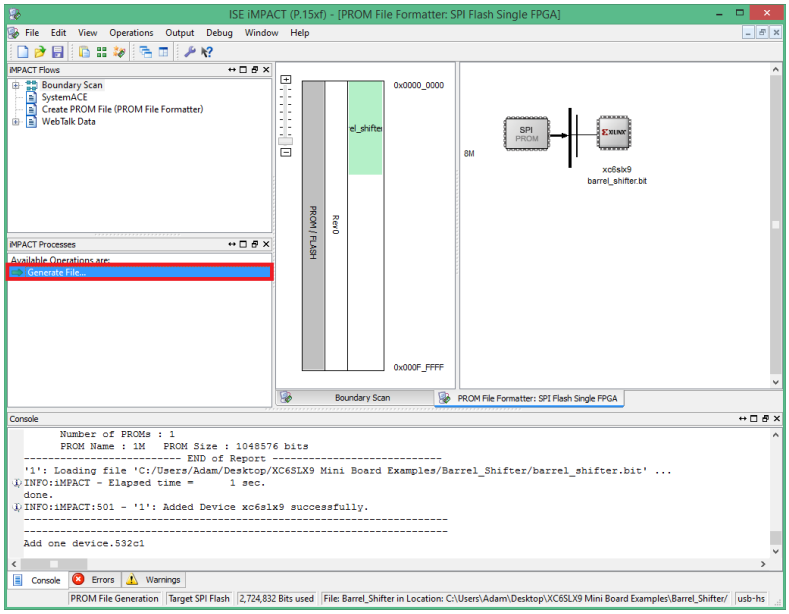
26) Select **Configure Single FPGA** in step1, 64M bit storage device in step 2, and change the **Output File Name** and **Output File Location** in step 3. Click **OK** to exit the setup window.



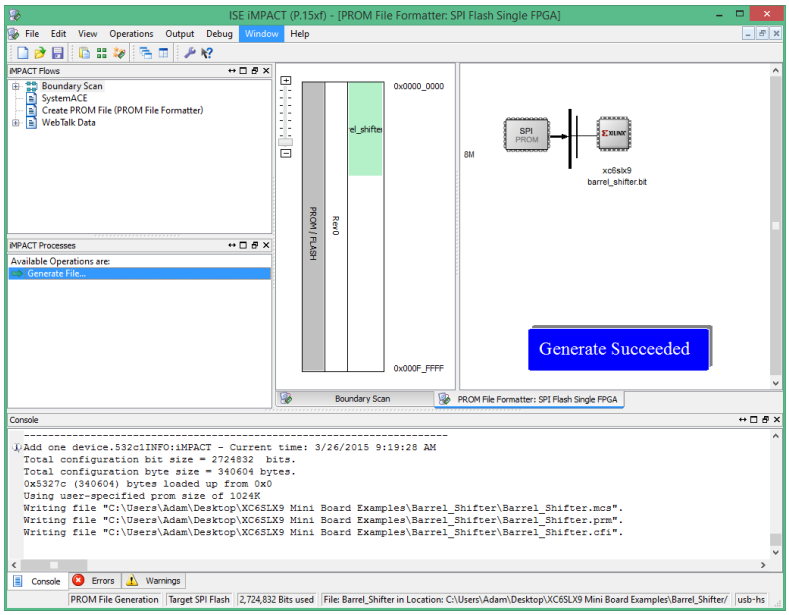
27) Add a device file as the source of this conversion. Locate the configuration file generated in previous steps.



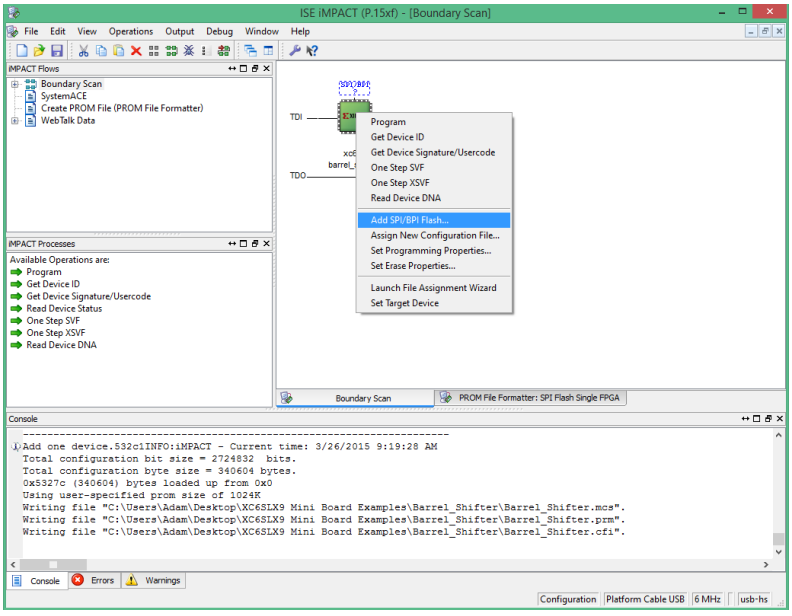
28) Double-click **Generate File...** command.



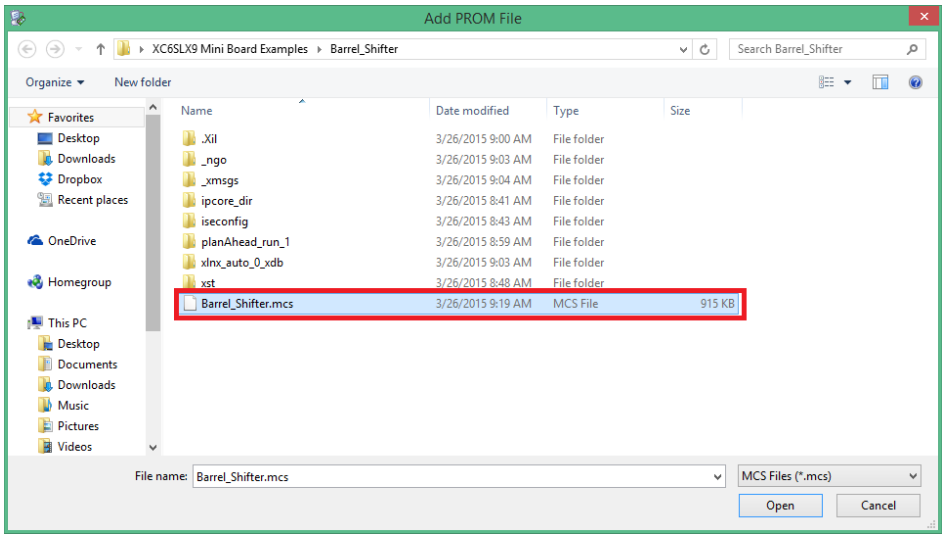
29) The Generate Succeeded message is displayed when file is converted successfully.



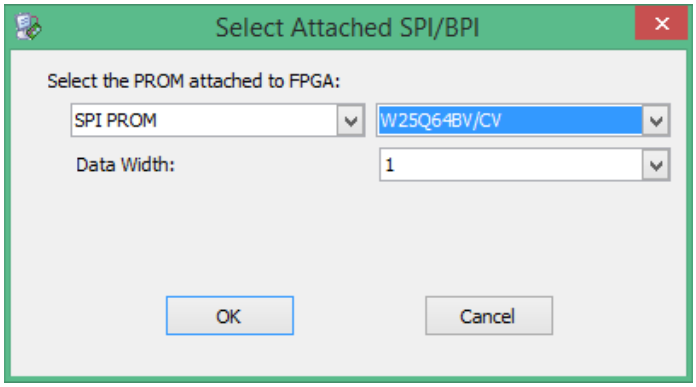
30) Go to the Boundary Scan window and right-click on the  icon, select **Add SPI/BPI flash...** command.



31) Locate the PROM file with .mcs suffix and click **Open**.

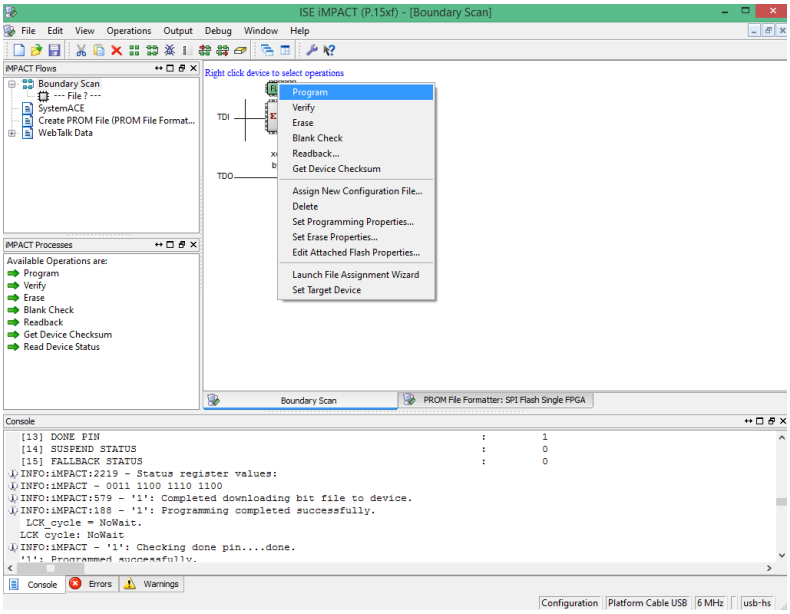


32) Select the SPI PROM(W25Q64BV) and Data Width as shown below. Click **OK** to exit.

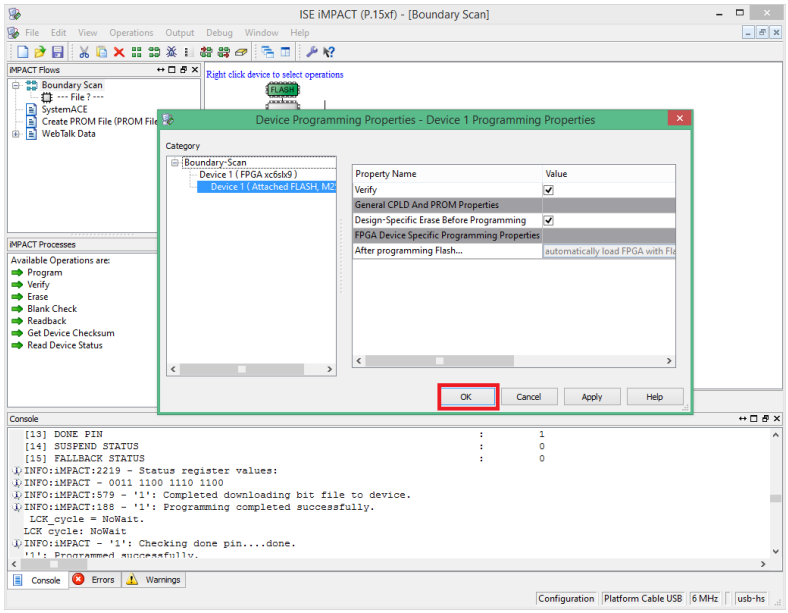


33) Right-click the 

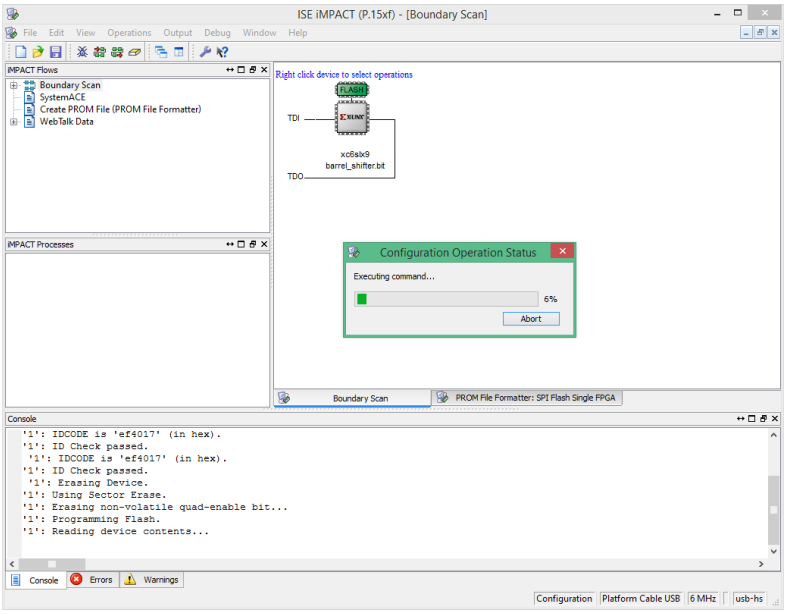
icon and select **Program** command to start programming the on-board SPI flash.



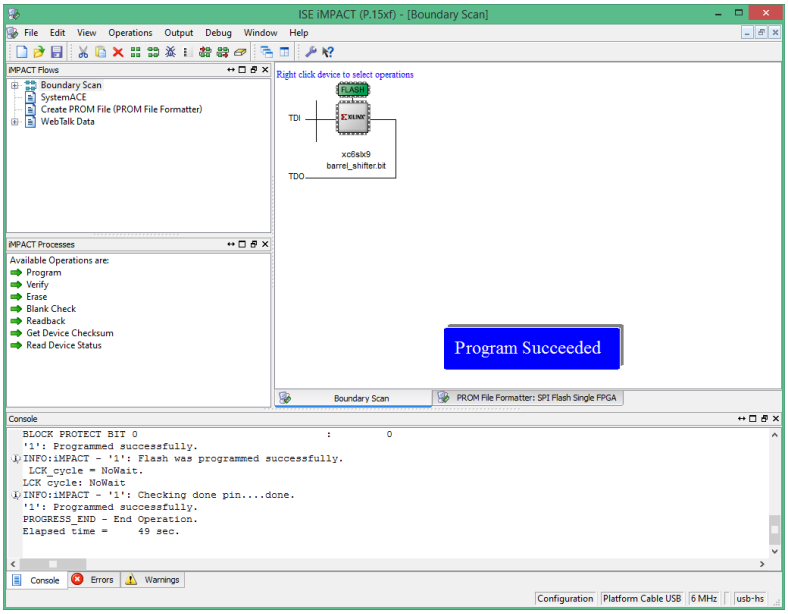
34) Click **OK** when Device Programming Properties window appears.



35) Wait patiently while programming the flash.



36) When programming is complete, the Program Succeeded message is displayed.



In this section, we learned the procedure of creating a simple FPGA project and verified it on XC6SLX9 Mini Board. Maybe it's a boring journey. But i really hope you have had a basic understanding of FPGA design using ISE WebPACK. If you want to learn more, please read the help documents and application notes on Xilinx website.

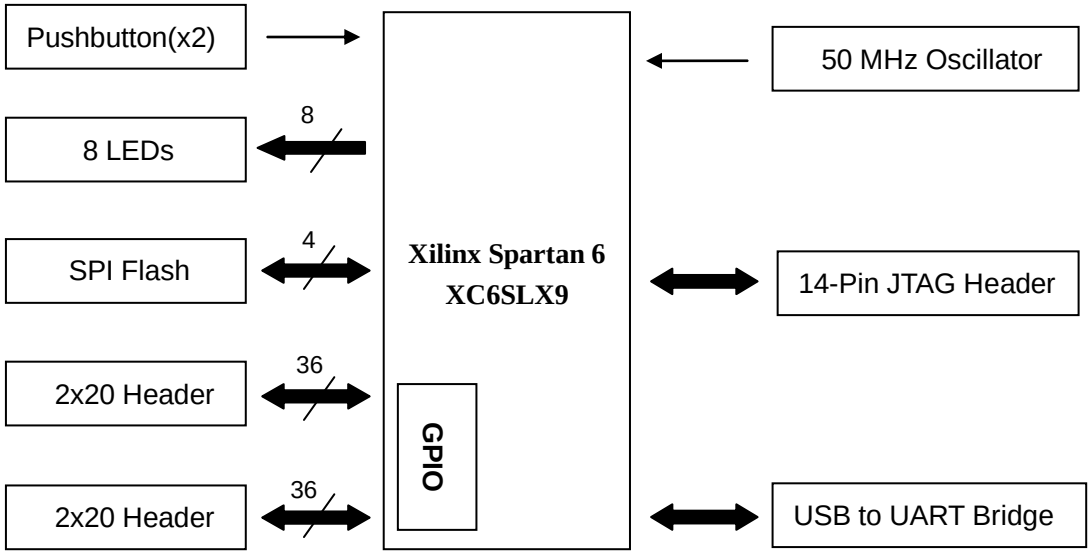
4. Hardware

This section describes the hardware peripherals of the XC6SLX9 Mini Board in detail.

Overview

The XC6SLX9 Mini Board is a pocket-sized platform for Xilinx Spartan 6 FPGA, it includes several basic components to learn digital design on FPGA.

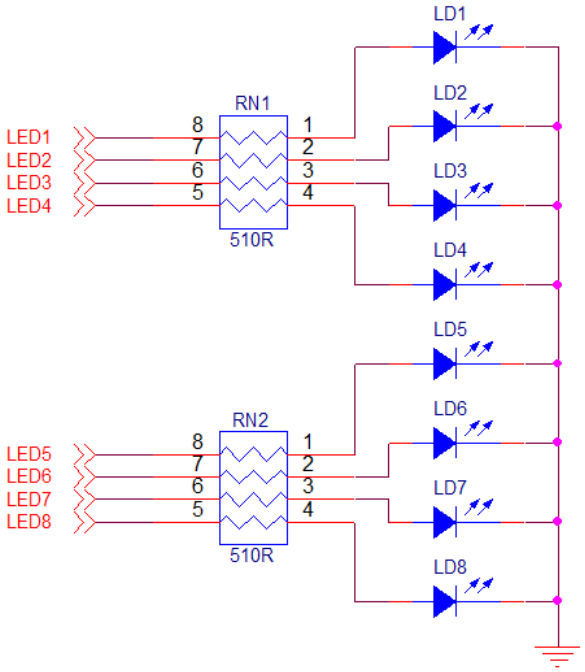
XC6SLX9 Mini Board Block Diagram



Peripherals and I/O Mapping

- **LEDs**

Eight LEDs are provided on this board. They are driven directly by the FPGA IOs. Setting one pin to high level lights the LED, and drive the pin low will turn it off. LEDs are usually used as status indicators. Also, eight LEDs can be used to display a 8-bit data.

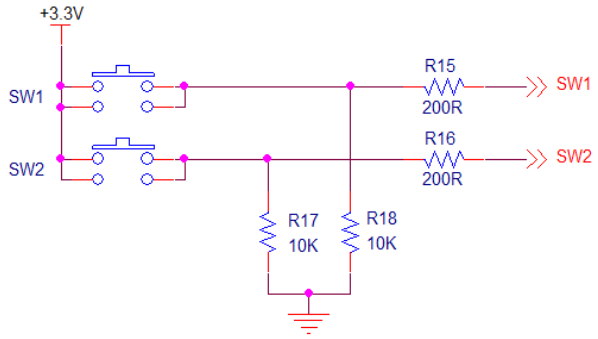


LED Interface

LED	FPGA Pin Location
LD1	138
LD2	137
LD3	134
LD4	133
LD5	120
LD6	119
LD7	118
LD8	117

- **Switches**

The XC6SLX9 Mini Board includes two pushbuttons for user input. Because of the characteristic of mechanical contact switch, glitches will be generated when button is pressed or released. You can implement a debounce circuit on FPGA to filter out the noise. A 200ohm resistor is added to protect IOs from overcurrent damage when pins are set as output in low level. In this case, when button pressed, +3.3V will be shorted to GND via the internal transistor path, and damage the output buffer. In default, the button keeps in low level state, when pressed, it will transit to high level state. Release the button the state will return to low level.

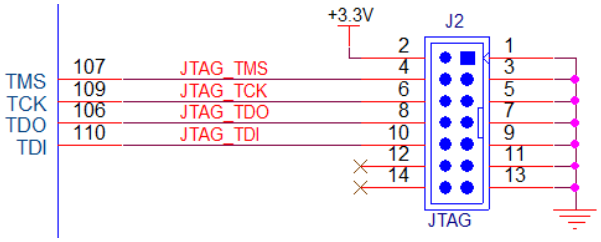


Switch Interface

Switch	FPGA Pin Number
SW1	132
SW2	131

- **JTAG**

The 14-Pin 2.54-Pitch JTAG header can be directly connected with a Xilinx download cable.

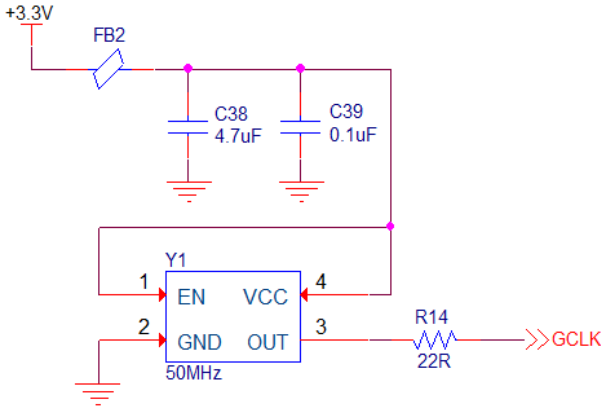


JTAG Interface

JTAG Connector Pin Number	JTAG Connector Pin Name	FPGA Pin Number	Pin Functionality
1	GND	—	GND
2	+3.3V	—	VCC
3	GND	—	GND
4	JTAG_TMS	107	TMS
5	GND	—	GND
6	JTAG_TCK	109	TCK
7	GND	—	GND
8	JTAG_TDO	106	TDO
9	GND	—	GND
10	JTAG_TDI	110	TDI
11	GND	—	GND
12	—	—	None
13	GND	—	GND
14	—	—	None

- **Clock Oscillator**

  Clock is an important element in synchronous digital circuit design. It's often used to synchronize the whole digital system. A 50 MHz oscillator is available on this board. You can use it as a global clock for your design or as a reference clock for internal PLL of FPGA.

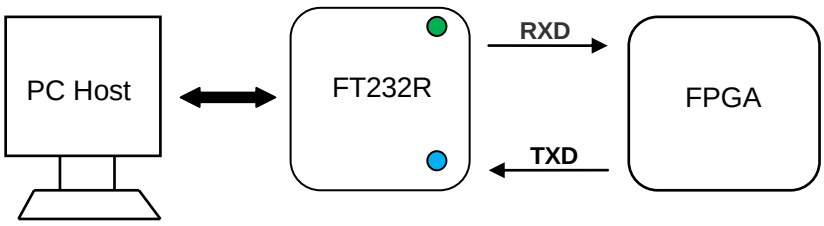


Clock Oscillator Interface

Clock Oscillator	FPGA Pin Number
Y1	50

- **USB to UART Bridge**

Serial communication can be easily implemented and is widely used when data exchange is needed between PC and peripherals. Since most new generation PCs are not assembled with an older 9-Pin D-Sub serial port. But USB port is abundant. The USB to UART converter IC solves the problem while retaining the advantage of serial port. FT232R is used in this board to play a role of USB to UART converter. When the driver software is properly installed, it will function as a virtual serial port. In addition, two LEDs are used to indicate the status of the TXD and RXD data path. When valid data transfer is detected, the corresponding LED will blink.

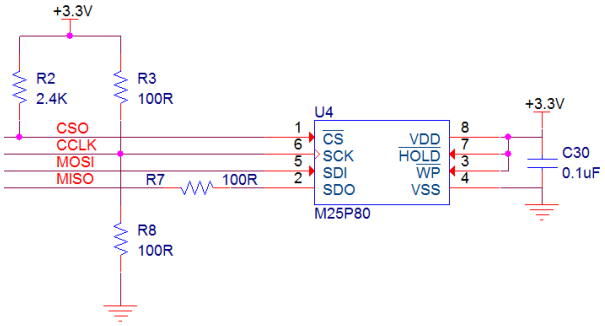


UART Interface

UART Signal Name	FPGA Pin Number
FPGA_RX	47
FPGA_TX	46

- **SPI Flash**

  The SPI flash on this board is intended to store FPGA configuration file. But it can also be used as a regular SPI flash if you like.



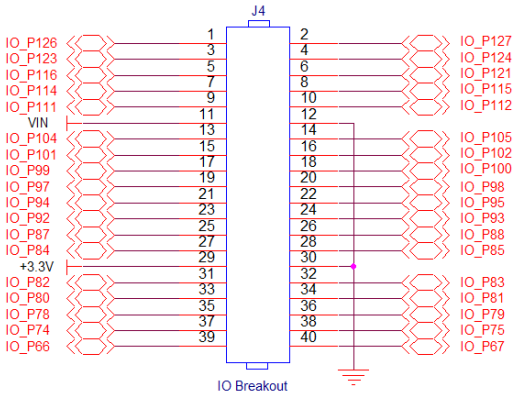
SPI Flash Interface

SPI Flash Signal Name	FPGA Pin Number
CSO	38
CCLK	70
MOSI	64
MISO	65

- **Expansion Header**

  Two groups of expansion header are available. Each header includes 36 I/Os and +5V, +3.3V power supply. The connector type is a 2x20 0.1" center-to-center, male.

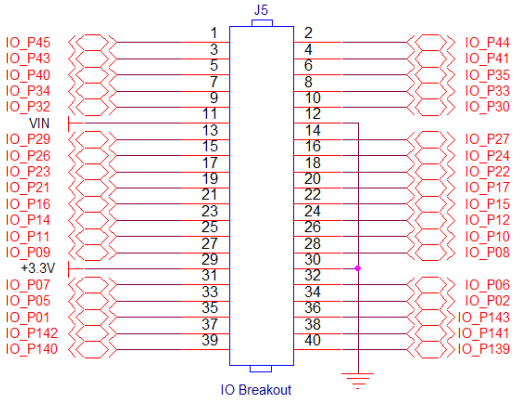
Header—J4 Interface



Expansion Connector Pin number	Expansion Connector Signal Name	FPGA Pin Number	Pin Functionality
1	IO_P126	126	I/O
2	IO_P127	127	I/O
3	IO_P123	123	I/O

4	IO_P124	124	I/O
5	IO_P116	116	I/O
6	IO_P121	121	I/O
7	IO_P114	114	I/O
8	IO_P115	115	I/O
9	IO_P111	111	I/O
10	IO_P112	112	I/O
11	VIN	—	Power
12	GND	—	Ground
13	IO_P104	104	I/O
14	IO_P105	105	I/O
15	IO_P101	101	I/O
16	IO_P102	102	I/O
17	IO_P99	99	I/O
18	IO_P100	100	I/O
19	IO_P97	97	I/O
20	IO_P98	98	I/O
21	IO_P94	94	I/O
22	IO_P95	95	I/O
23	IO_P92	92	I/O
24	IO_P93	93	I/O
25	IO_P87	87	I/O
26	IO_P88	88	I/O
27	IO_P84	84	I/O
28	IO_P85	85	I/O
29	+3.3V	—	Power
30	GND	—	Ground
31	IO_P82	82	I/O
32	IO_P83	83	I/O
33	IO_P80	80	I/O
34	IO_P81	81	I/O
35	IO_P78	78	I/O
36	IO_P79	79	I/O
37	IO_P74	74	I/O
38	IO_P75	75	I/O
39	IO_P66	66	I/O
40	IO_P67	67	I/O

Header—J5 Interface



Expansion Connector Pin number	Expansion Connector Signal Name	FPGA Pin Number	Pin Functionality
1	IO_P45	45	I/O
2	IO_P44	44	I/O
3	IO_P43	43	I/O
4	IO_P41	41	I/O
5	IO_P40	40	I/O
6	IO_P35	35	I/O
7	IO_P34	34	I/O
8	IO_P33	33	I/O
9	IO_P32	32	I/O
10	IO_P30	30	I/O
11	VIN	—	Power
12	GND	—	Ground
13	IO_P29	29	I/O
14	IO_P27	27	I/O
15	IO_P26	26	I/O
16	IO_P24	24	I/O
17	IO_P23	23	I/O
18	IO_P22	22	I/O
19	IO_P21	21	I/O
20	IO_P17	17	I/O
21	IO_P16	16	I/O
22	IO_P15	15	I/O
23	IO_P14	14	I/O
24	IO_P12	12	I/O
25	IO_P11	11	I/O
26	IO_P10	10	I/O
27	IO_P09	09	I/O

28	IO_P08	08	I/O
29	+3.3V	—	Power
30	GND	—	Ground
31	IO_P07	07	I/O
32	IO_P06	06	I/O
33	IO_P05	05	I/O
34	IO_P02	02	I/O
35	IO_P01	01	I/O
36	IO_P143	143	I/O
37	IO_P142	142	I/O
38	IO_P141	141	I/O
39	IO_P140	140	I/O
40	IO_P139	139	I/O

Revision History

Revision	Date	Note
REV. 0	10/1/2014	Initial release
REV. 1	4/1/2015	Upgrade the on-board SPI flash M25P80 to W25Q64BV.

Thank You !