Developer : Mitu Raj
Mail ID : *iammituraj@gmail.com*

SPI Master IP Core

- *A Portable Soft IP Core, version 1.0*
- *An Open Source Design*

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Specifications

SPI Master v.1.0 is an IP Core for SPI Master for low/medium speed serial communication with SPI slave peripherals.

- Supports all four modes of SPI; dynamically configurable
- Clock Enable control for power saving
- Statically configurable word length and SPI Clock speed
- MSb to LSb bit-order transmission
- Single interrupt for transmission and reception
- SPI Clock speed supported up to 50 MHz
- Source synchronous interface with in-built synchronisers
- Bare RTL design,

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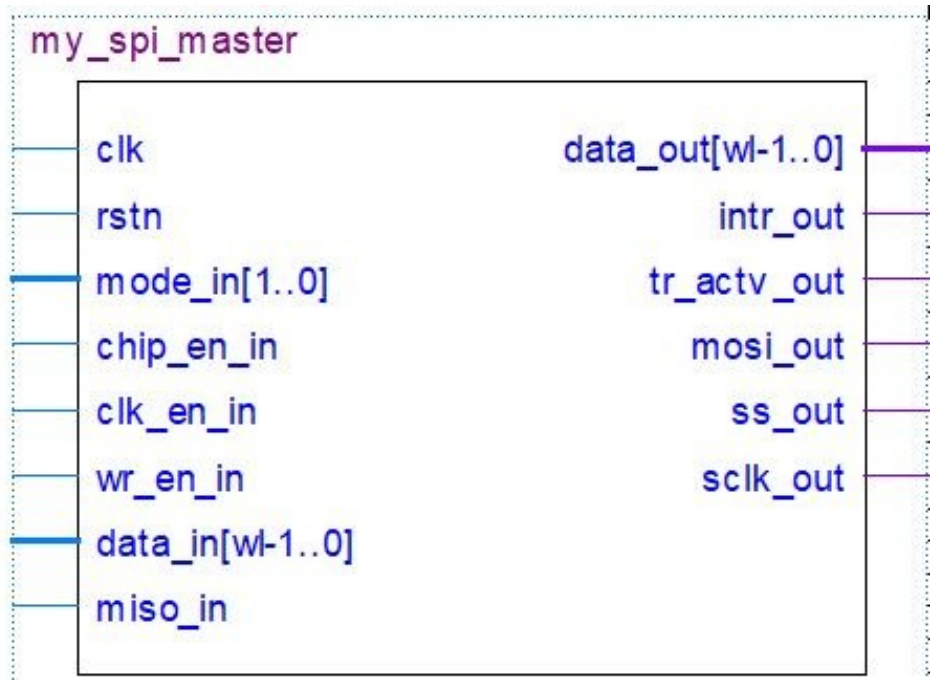
RTL Schematic



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Configurable Parameters

Parameter	Description
WL	Data bus width
DV	Clock Division Factor

Ports

Signal	Direction	Width	Description
clk	in	1	Clock
rstn	in	1	Async reset **
mode_in	in	2	To choose mode of SPI operation
chip_en_in	in	1	Chip Enable to start a transaction
clk_en_in	in	1	Clock enable to start internal clock
wr_en_in	in	1	Write Enable to start SPI data communication
data_in	in	WL-1	Data word to be transmitted on MOSI line
miso_in	in	1	Serial Data In
data_out	out	WL-1	Data word received on MISO line
intr_out	out	1	Interrupt signal
tr_actv_out	out	1	Transaction status **
mosi_out	out	1	Serial Data Out
ss_out	out	1	Slave Select **
sclk_out	out	1	Serial SPI Clock

*** Active-low signals*

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SPI Transaction

Following steps are followed to initiate an SPI transaction with the SPI Master IP.

1. Reset the IP.
2. Set the Mode of SPI operation.
3. Assert Clock Enable to start the internal spi clock.
4. Assert Chip Enable to select the slave.
5. Update Transmit-Data-Word and pull Write Enable high in the next cycle. This will start SPI data communication.
6. Pull Write Enable low when Interrupt goes low.
7. Interrupt goes high once the the data word is fully transmitted. Received data word can be read at this point.
8. Repeat steps 5 to 7, until the transaction needs to be stopped.
9. De-assert Chip Enable to stop the on-going transaction.
10. De-assert Clock Enable when Transaction-Active-Status goes high.

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SCLK speed

Serial SPI Clock (SCLK) speed can be configured statically using ***DV*** parameter. The expression for SCLK is given below:

$$SCLK = \frac{\boldsymbol{clk}}{(\boldsymbol{DV}*4)}$$

Maximum speed is hence one-fourth of the global clock, ***clk***.

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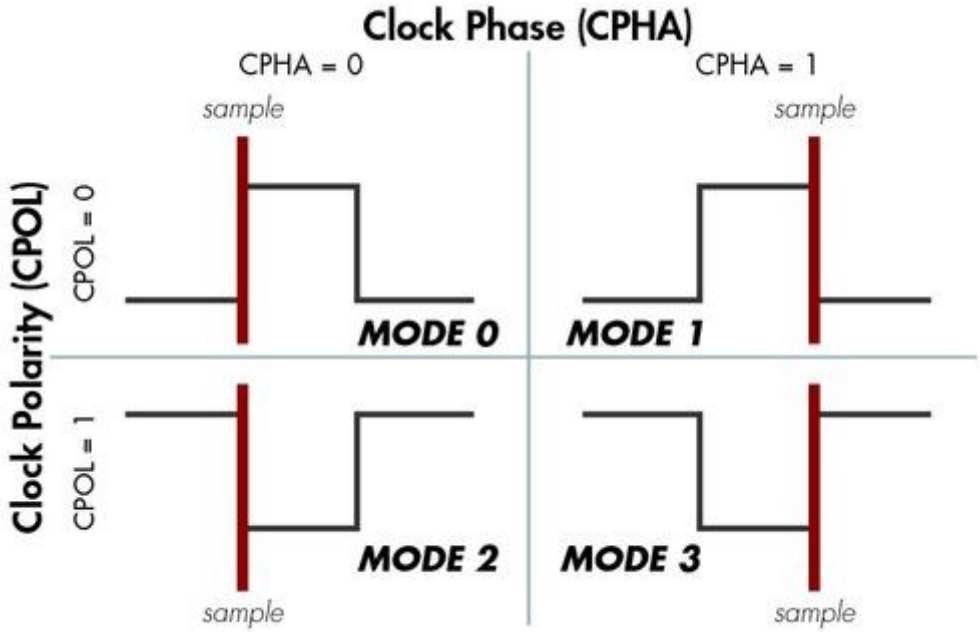
SPI Modes



mode_in	**Description**
00	Mode 0
01	Mode 1
10	Mode 2
11	Mode 3

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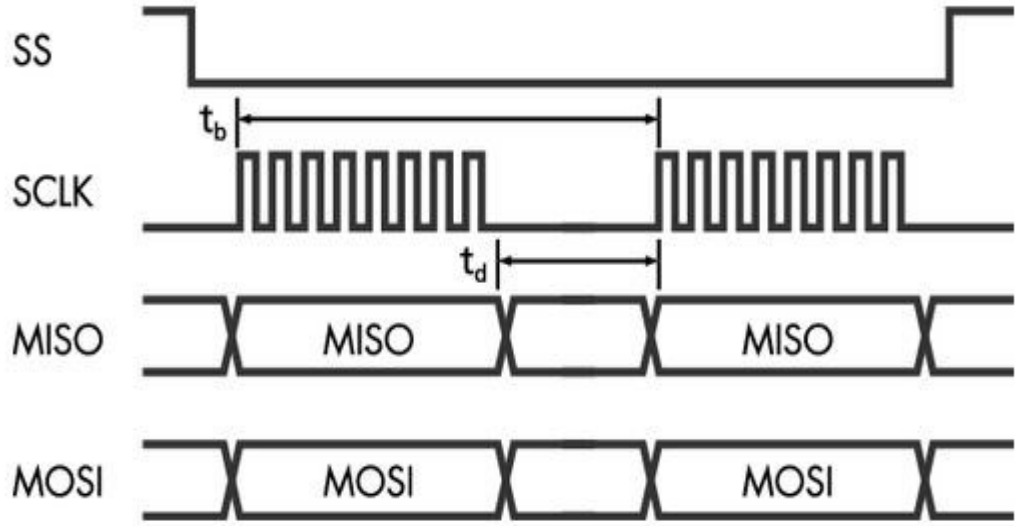
Timing



Parameter	No. of SCLK cycles (Typical)
SS assertion to first SCLK edge	2 *
Last SCLK edge to SS de-assertion	2 **
Setup time (Inter-frame delay td)	2 **

** in-code configurable*

*** controllable by user dynamically*

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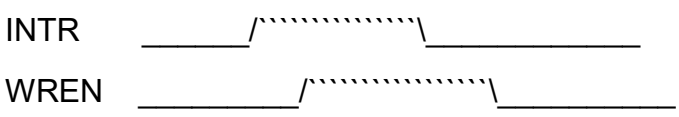
Handshaking protocol

Following timing diagram shows basic handshaking between Interrupt signal and Write Enable between data frames.



Write Enable is pulsed high and low depending on Interrupt's current state.

Important Notes

- To change the SPI Mode and start a new transaction, the on-going transaction has to be stopped, and Clock Enable has to be de-asserted. Or change the Mode and reset the IP.
- Not pulsing Write Enable after a data word transmission, will cause the SCLK to remain in its idle state until its pulsed.
- Pulling Clock Enable low during an ongoing transaction will delay the transmission.
- Known limitations: Since no PLL or dedicated clock generators are not used, within FPGA and for external applications, recommended SCLK speed is < 25 MHz. This ensures minimal clock slew degradation.

Notice

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