

INSTITUTE OF SPACE TECHNOLOGY ISLAMABAD

Department of Electrical Engineering

Digital Logic Design LAB



Institute of
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Project Report

Batch/Sec: EE20-A

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Project Title: ODD NUMBER UP/DOWN COUNTER [0-99]

Objective:

In this digital logic design project, made a 2-digit odd counter using D-Flip Flops. This counter has features like:

- Up Counting
- Down Counting
- Reset option

Components:

The components used in a project,

- D-Flip Flop ICs
- AND Gate ICs
- OR Gate ICs
- NOT Gate ICs
- XOR Gate ICs
- 555 timer IC
- Resistors
- Capacitors
- 7-Segment Displays
- Binary to Seven Segment Decoder ICs
- BCD Counter ICs
- Push Button
- Toggle Switch
- Jumper Wires
- Bread Board

Theory:

A D flip-flop is a digital circuit element used for storing binary data in sequential logic systems. It has a clock input, a data input (D), and outputs a single binary value representing the stored data. The flip-flop's state changes on the rising or falling edge of the clock signal, allowing synchronized storage and retrieval of information.

AND gate: A digital logic gate that produces a high output only when all of its inputs are high, representing the logical AND operation.

OR gate: A digital logic gate that produces a high output if at least one of its inputs is high, representing the logical OR operation.

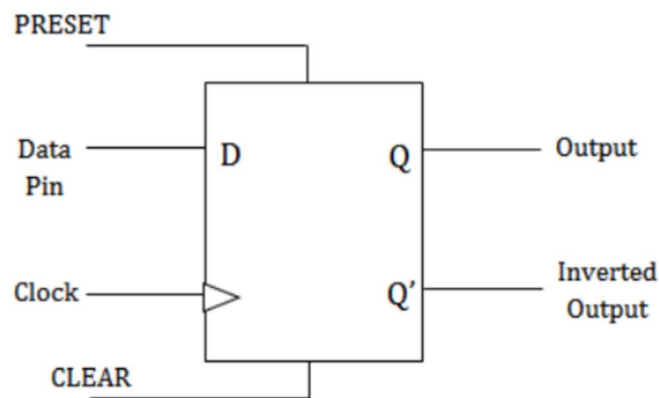
NOT gate: A digital logic gate that produces an output that is the inverse (complement) of its input, representing the logical NOT operation.

The 555 timer is an integrated circuit widely used in electronics for generating accurate time delays or oscillations. It comprises two voltage comparators, a flip-flop, a discharge transistor, and a resistor divider network.

A seven-segment display is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot matrix displays.

Counters in Digital Logic Design (DLD) are sequential logic circuits that generate a series of binary numbers in a specific order. They typically consist of flip-flops and combinational logic to create a counting sequence based on clock pulses.

Decoders in Digital Logic Design (DLD) are combinational circuits that convert coded inputs into a unique output line. They are commonly used to enable specific functions based on the input code, facilitating the selection of a particular output in a larger system. Decoders play a crucial role in applications like memory addressing, where they decode binary addresses to activate specific memory locations.



Symbol: D Flip-flop

Procedure & Working:

Step 1: States

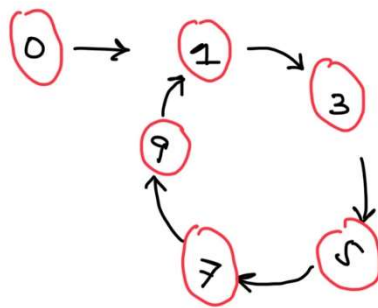
First of all we will write down all the states for our counter. That is how our odd counter using D-Flip Flops will initiate and continue. To make a 2-digit odd up and down counter we need an enable bit and only need to change the 1st digit on one's decimal place to odd number. That is the counter starts from 0 and then goes to 1,3,5,7,9 and then again at 1 not zero i.e. because it's an odd counter and vice versa. Now for the tens decimal place we will use simple BCD counter IC to count from 0 to 9 or 9 to zero, the clock for this IC will come from the odd counter, basically we will cascade 1 BCD counter with the ODD up-down counter.

DLD ODD UP & DOWN COUNTER

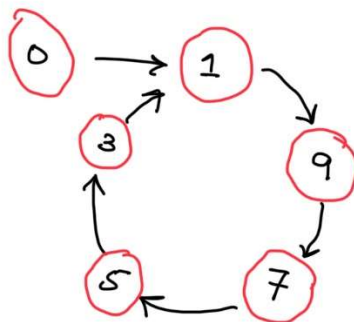
⇒ Since we are making an up & down counter, this means we must have an enable bit to control Up & Down counting of counter.

EN bit
0 ⇒ UP Counter

States



EN Bit
1 ⇒ Down Counter



Step 2: Truth Table

Now the next step is writing the truth table and logic for make the ODD counter work. We achieve this goal as shown in the picture above. Now we know what the inputs for the D-Flip Flops should be.

TRUTH TABLE :

PRESET STATE					NEXT STATE					Flip Flop INPUTS			
EN	B	C	D	E	B	C	D	E	D ₄	D ₃	D ₂	D ₁	
0	0	0	0	0	0	0	0	1	0	0	0	1	
0	0	0	0	1	0	0	1	1	0	0	1	1	
0	0	0	1	1	0	1	0	1	0	1	0	1	
0	0	1	0	1	0	1	1	1	0	1	1	1	
0	0	1	1	1	1	0	0	1	1	0	0	1	
0	1	0	0	1	0	0	0	1	0	0	0	1	
1	0	0	0	0	1	0	0	1	1	0	0	1	
1	1	0	0	1	0	1	1	1	0	1	1	1	
1	0	1	1	1	0	1	0	1	0	1	0	1	
1	0	1	0	1	0	0	1	1	0	0	1	1	
1	0	0	1	1	0	0	0	1	0	0	0	1	
1	0	0	0	1	1	0	0	1	1	0	0	1	

Step 3: Karnaugh Map

In the next step we will use the truth table to write down the Karnaugh map to get the logic gate equations so that we can implement our counter using the ICs. K-map is solved in the picture above.

Now K-MAPS

D_4

EN, B, C	DE			
	00	01	11	10
000	0	0	0	X
001	X	0	1	X
011	X	X	X	X
010	X	0	X	X
100	1	1	0	X
101	X	0	0	X
111	X	X	X	X
110	X	0	X	X

$$D_4 = \overline{E_n} C D + E_n \overline{B} \overline{C} \overline{D}$$

D_3

EN, B, C	DE			
	00	01	11	10
000	0	0	1	X
001	X	1	0	X
011	X	X	X	X
010	X	0	X	X
100	0	0		X
101	X	0	1	X
111	X	X	X	X
110	X	1	X	X

$$D_3 = E_n B + \overline{E_n} \overline{C} \overline{D} + \overline{E_n} C \overline{D} + E_n C D$$

D_2

EN, B, C	DE			
	00	01	11	10
000	0	1	0	X
001	X	1	0	X
011	X	X	X	X
010	X	0	X	X
100	0	0	0	X
101	X	1	0	X
111	X	X	X	X
110	X	1	X	X

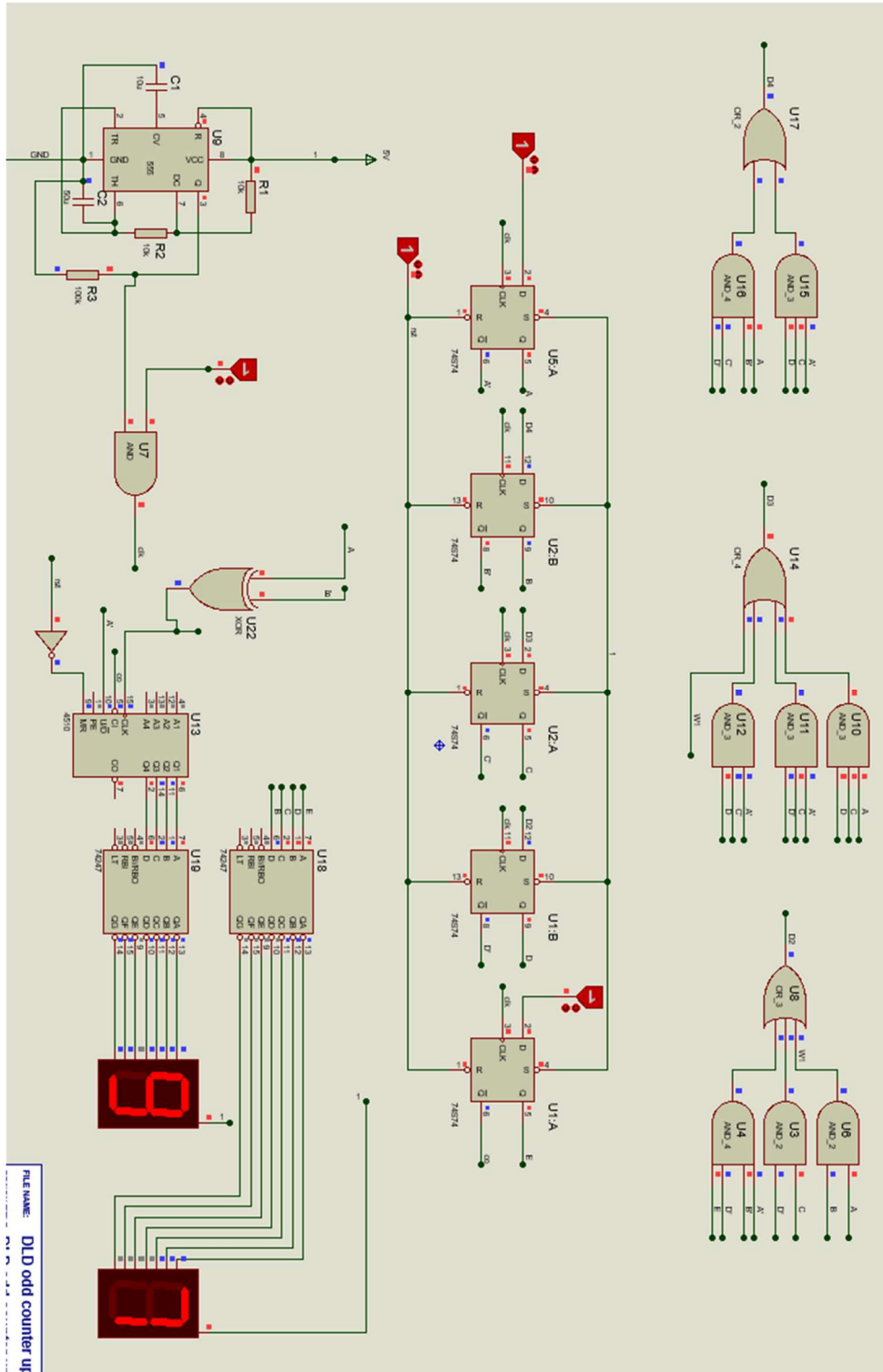
$$D_2 = C\bar{D} + E_n B + \bar{E}_n \bar{B} \bar{D} E$$

$$D_1 = 1$$

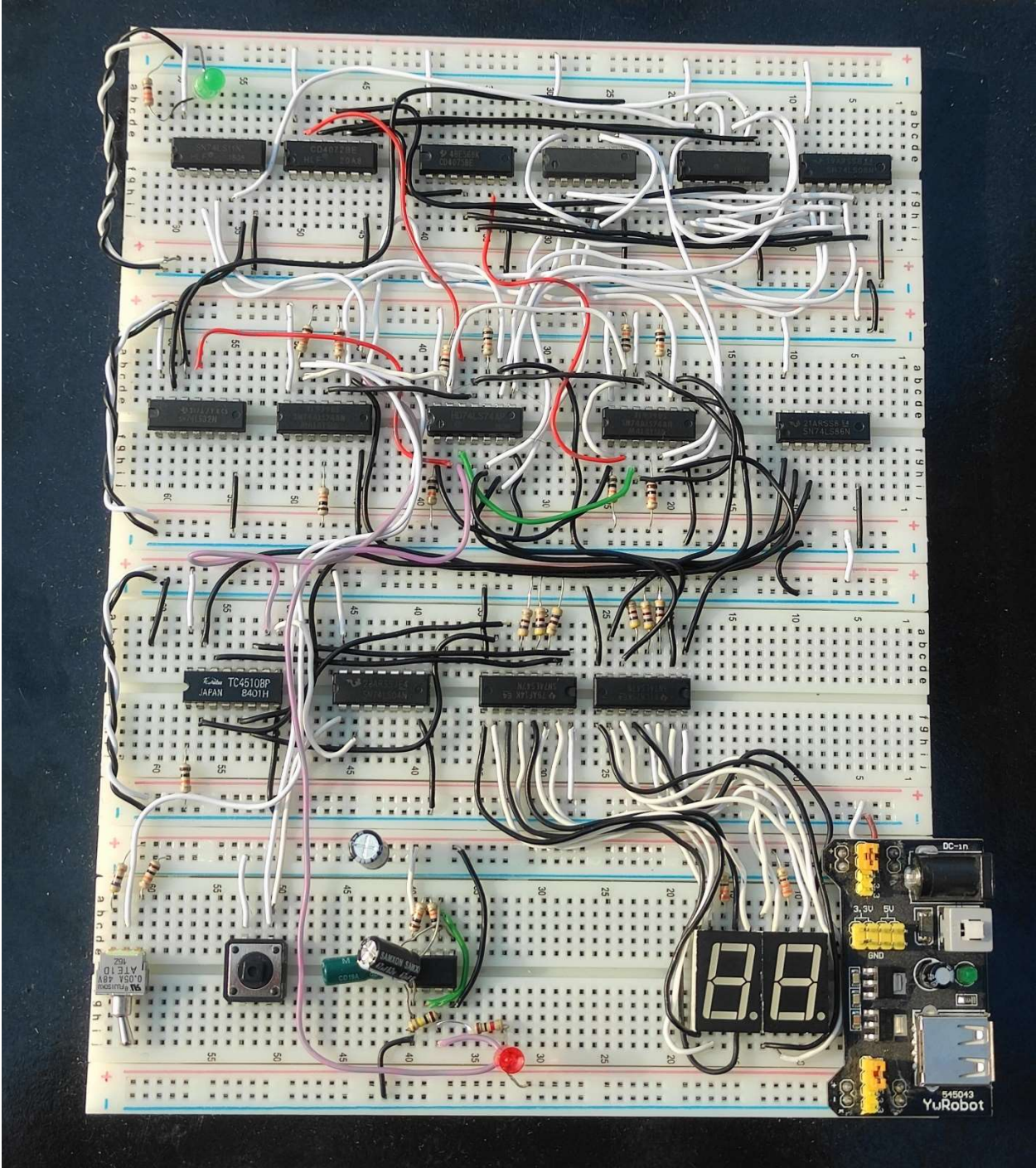
We can see from the table that D_1 is always 1.

Step 4: Simulation

In this step we will use the truth table to write down the Karnaugh map to get the logic gate equations so that we can implement our counter using the ICs.



Step 5: Hardware



What did we learn?

We learn that how the digital meters and counters work by using of 7-segment displays, D flipflops, Counters etc.

Conclusion:

We conclude that The project "ODD Numbers Counter from 0 to 99" in Digital Logic Design (DLD) utilizes counters and flip-flops to sequentially count and display odd numbers within the range of 0 to 99. A binary counter is employed to increment through the numbers, while a D flip-flop is utilized to identify and filter odd values. This implementation leverages combinational and sequential logic to achieve an efficient and systematic counting mechanism, ensuring accurate representation and tracking of odd numbers within the specified range.