I²C Bus Control Broadband Video Switch
Monolithic IC MM1630

Outline

This is a video switch IC with I²C bus control developed for high-resolution TVs, PDP and projection TVs. It can switch 4 color difference signal lines (component signals), 5 S-video signal lines and 8 composite signal lines.
Design of the input switch block can be simplified by using this IC with MM1631 (audio switch IC).

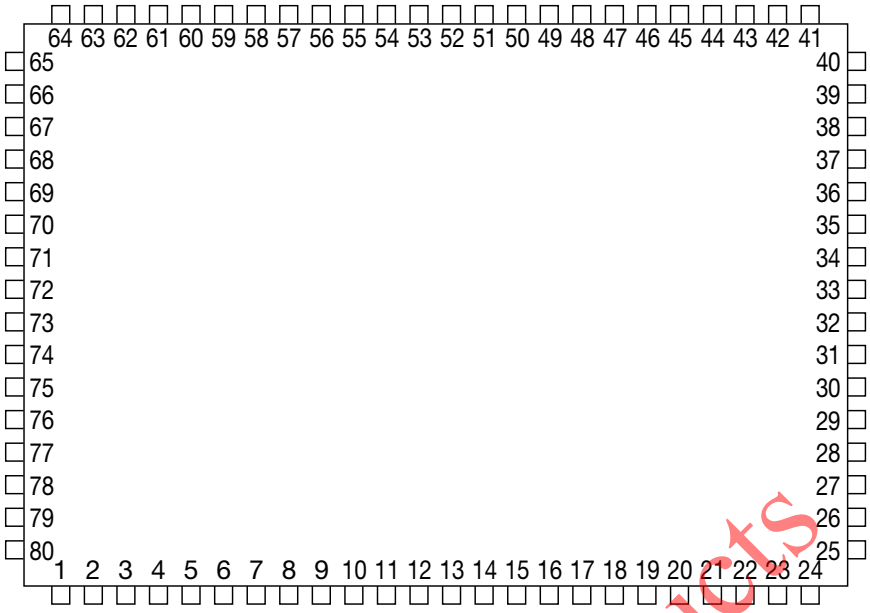
Features

1. Supports component signals (enables 4-input switching and 5-input S-video signal switching) frequency response: 50MHz
2. Enables 8-input switching of component signals
3. Serial control by I2C bus
4. Includes a 0dB/6dB switching amp (OUT1/OUT2/OUT4)
5. Includes a filter (13.5MHz LPF) (slew selection possible)
6. Includes D-pin detection and S-pin detection functions
7. The $V_{OUT}3$, $Y_{OUT}3$, and $C_{OUT}3$ pins support 75Ω drive.

Package

QFP-80D

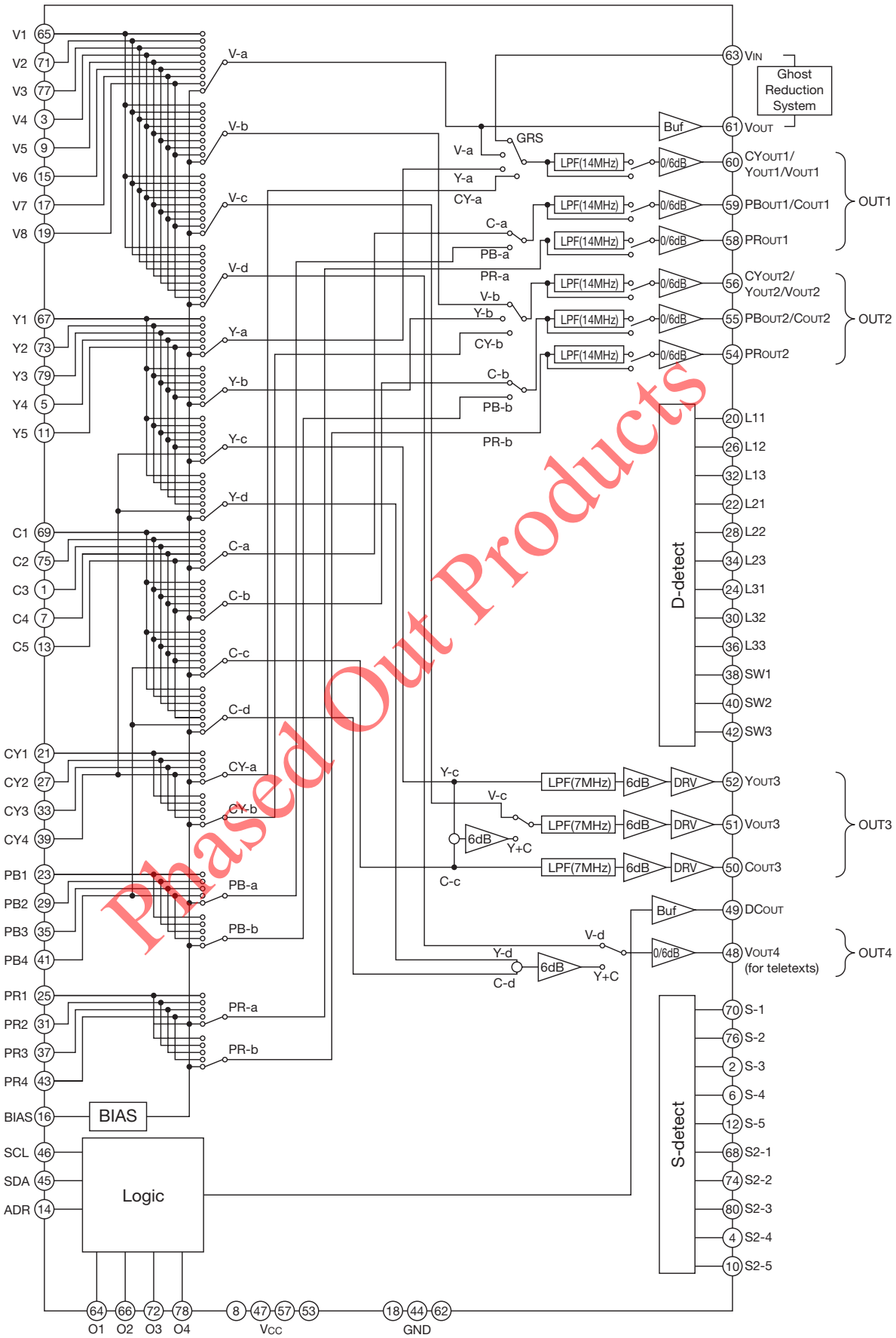
Pin Assignment



QFP-80D
(TOP VIEW)

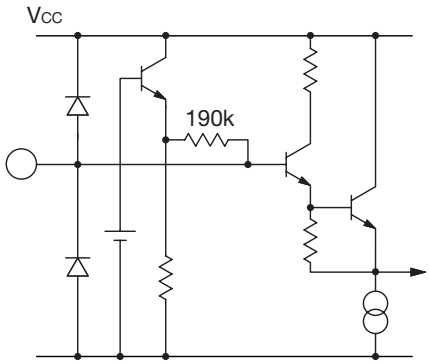
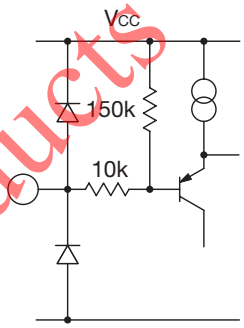
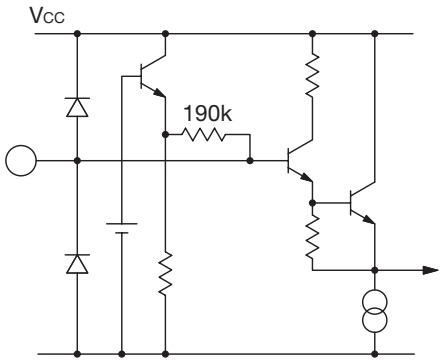
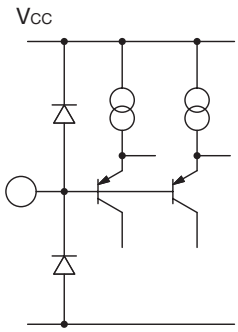
1	C3	17	V7	33	CY3	49	DCOUT	65	V1
2	S-3	18	GND	34	L23	50	COUT3	66	O2
3	V4	19	V8	35	PB3	51	VOUT3	67	Y1
4	S2-4	20	L11	36	L33	52	YOUT3	68	S2–1
5	Y4	21	CY1	37	PR3	53	VCC	69	C1
6	S-4	22	L21	38	SW1	54	PROUT2	70	S–1
7	C4	23	PB1	39	CY4	55	PBOUT2/COUT2	71	V2
8	VCC	24	L31	40	SW2	56	CYOUT2/YOUT2/VOUT2	72	O3
9	V5	25	PR1	41	PB4	57	VCC	73	Y2
10	S2–5	26	L12	42	SW3	58	PROUT1	74	S2–2
11	Y5	27	CY2	43	PR4	59	PBOUT1/COUT1	75	C2
12	S-5	28	L22	44	GND	60	CYOUT1/YOUT1/VOUT1	76	S–2
13	C5	29	PB2	45	SDA	61	VOUT	77	V3
14	ADR	30	L32	46	SCL	62	GND	78	O4
15	V6	31	PR2	47	VCC	63	VIN	79	Y3
16	BIAS	32	L13	48	VOUT4	64	O1	80	S2–3

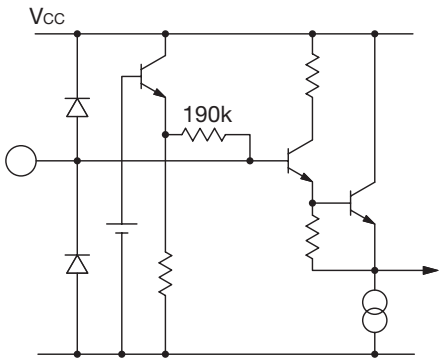
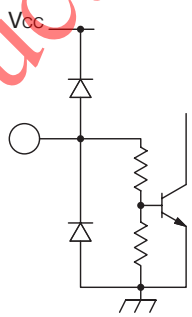
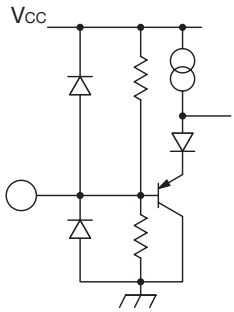
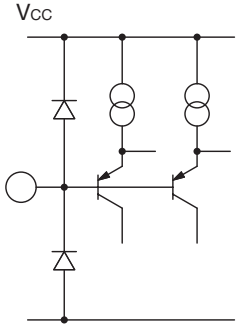
Block Diagram

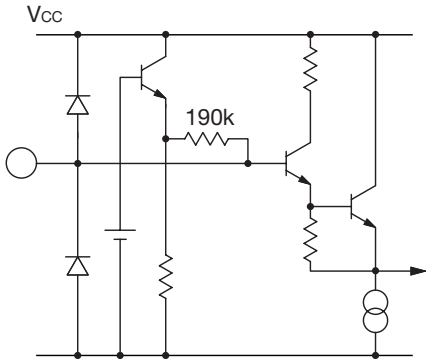
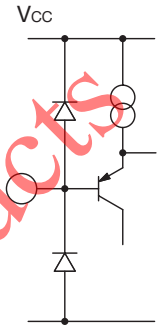
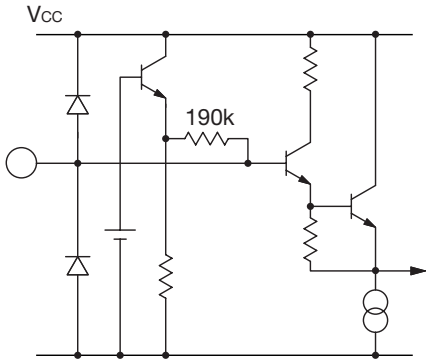
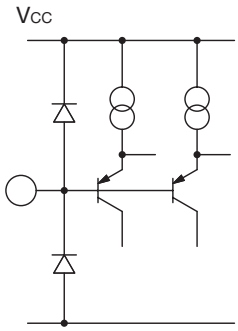


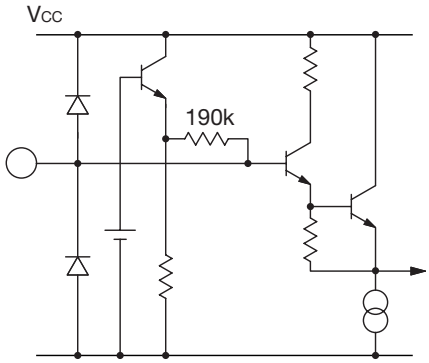
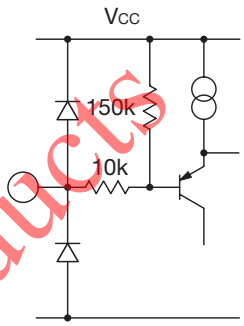
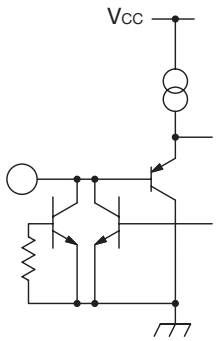
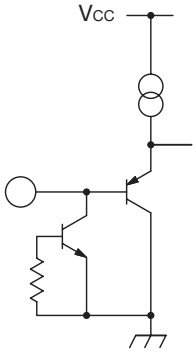
Note: Only OUT3 can correspond to 75Ω drive.

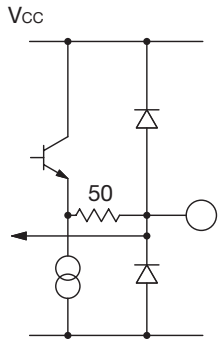
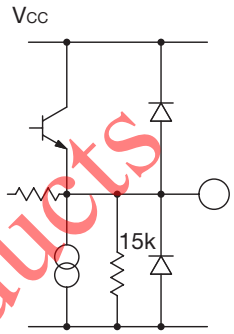
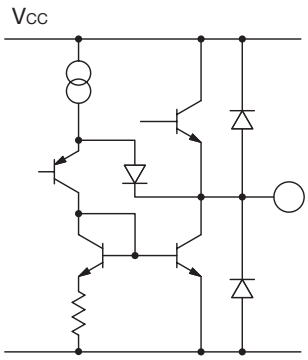
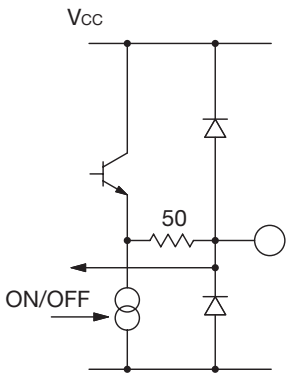
Pin Description

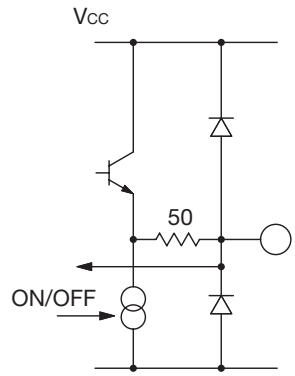
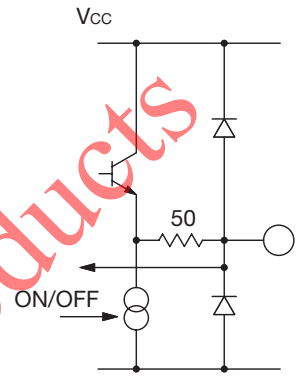
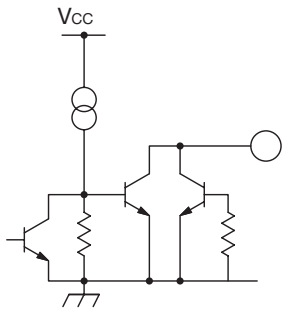
Pin no.	Pin name	Functions	Internal equivalent circuit diagram
1 7 13 69 75	C3 C4 C5 C1 C2	Croma signal input	
2 6 12 70 76	S–3 S–4 S–5 S–1 S–2	SW of S connector	
3 9 15 17 19 63 65 71 77	V4 V5 V6 V7 V8 V_{IN} V1 V2 V3	Composite signal input	
4 10 68 74 80	S2–4 S2–5 S2–1 S2–2 S2–3	Detect of S connector	

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
5 11 67 73 79	Y4 Y5 Y1 Y2 Y3	Luminance signal input	
8 47 53 57	Vcc	Vcc	
14	ADR	Slave address select PIN	
16	BIAS	Bias	
18 44 62	GND	GND	
20 26 32	L11 L12 L13	Detect of D connector scanning line	

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
21 27 33 39	CY1 CY2 CY3 CY4	Color difference signal input	
22 28 34	L21 L22 L23	Detect of D connector I/P	
23 29 35 41	PB1 PB2 PB3 PB4	Color difference signal input	
24 30 36	L31 L32 L33	Detect of D connector aspect	

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
25 31 37 43	PR1 PR2 PR3 PR4	Color difference signal input	
38 40 42	SW1 SW2 SW3	SW of D connector	
45	SDA	Data input of I²C BUS	
46	SCL	CLK input of I²C BUS	

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
48 61	VOUT4 VOUT	Composite signal output for teletexts Composite signal output for GRS *GRS Ghost Reduction System	
49	DCOUT	S - DCOUT	
50 51 52	COUT3 VOUT3 YOUT3	Monitor output	
54 58	PROUT2 PROUT1	Color difference signal output	

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
55 59	PBOUT2/COUT2 PBOUT1/COUT1	Color difference signal or Croma signal output	
56 60	CYOUT2/YOUT2/VOUT2 CYOUT1/YOUT1/VOUT1	Color difference signal, Luminance signal or Composite signal output	
64 66 72 78	O1 O2 O3 O4	Output port 1~4	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	–65~+150	°C
Operating temperature	T_{OPR}	–40~+85	°C
Supply voltage	V_{CC} max.	–0.2~+13	V
Input voltage	V_{IN} max.	–0.2~V_{CC}+0.2	V
Output voltage	V_{OUT} max.	–0.2~V_{CC}+0.2	V
Output current	I_{OUT} max.	25	mA
Junction temperature	Tj max.	150	°C
Thermal resistance	θ j-c	6.0	°C/W
Allowable loss *1	Pd	3.6	W

Note: *1 Board mounting power dissipation. Board size 193×189×1.6mm

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	–40~+85	°C
Operating voltage	V_{CCOP}	+8.0~+10.0	V

Electrical Characteristics (Except where noted otherwise, Ta=25°C, V_{CC}=9V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption						
Current consumption	I_{CC0}	No signal OUT1 & OUT2 Power Save bit "0"	110	155	200	mA
Current of power save 1	I_{CC1}	No signal OUT1 Power Save bit "0" OUT2 Power Save bit "1" or OUT1 Power Save bit "1" OUT2 Power Save bit "0"	90	130	170	mA
Current of power save 2	I_{CC2}	No signal OUT1 & OUT2 Power Save bit "1"	70	100	130	mA
Input pin voltage						
Composite video signal input	V_{VIN}	3, 9, 15, 17, 19, 63, 65, 71, 77 PIN	5.1	5.5	5.9	V
Luminance signal input	V_{YIN}	5, 11, 67, 73, 79 PIN	5.1	5.5	5.9	V
Croma signal input	V_{CIN}	1, 7, 13, 69, 75 PIN	5.1	5.5	5.9	V
Color difference signal input 1	V_{CYIN}	21, 27, 33, 39 PIN	5.1	5.5	5.9	V
Color difference signal input 2	V_{PbIN}	23, 29, 35, 41 PIN	5.1	5.5	5.9	V
Color difference signal input 3	V_{PrIN}	25, 31, 37, 43 PIN	5.1	5.5	5.9	V
Output pin voltage						
Composite video signal output	V_{VOUT}	48, 51, 61 PIN	3.4	3.8	4.2	V
Luminance signal output	V_{YOUT}	52 PIN	3.4	3.8	4.2	V
Croma signal output	V_{COUT}	50 PIN	3.4	3.8	4.2	V
Color difference signal output 1	V_{CYOUT}	56, 60 PIN	3.4	3.8	4.2	V
Color difference signal output 2	V_{PbOUT}	55, 59 PIN	3.4	3.8	4.2	V
Color difference signal output 3	V_{PrOUT}	54, 58 PIN	3.4	3.8	4.2	V

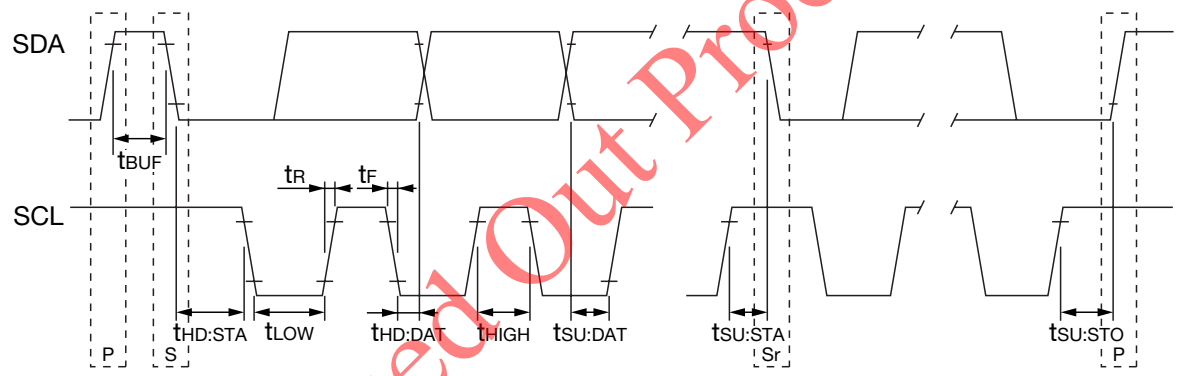
Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
S-DCOUT pin output voltage							
S-DCOUT PIN output voltage	L	VDCOUT L	49 PIN RL=10kΩ+100kΩ		0.1	0.5	V
	M	VDCOUT M	49 PIN RL=10kΩ+100kΩ	1.6	2.1	2.4	V
	H	VDCOUT H	49 PIN RL=10kΩ+100kΩ	4.3	4.6		V
Input impedance							
VIN input impedance		ZVIN	3, 9, 15, 17, 19, 63, 65, 71, 77 PIN	135	190	250	kΩ
YIN input impedance		ZYIN	5, 11, 67, 73, 79 PIN	135	190	250	kΩ
CIN input impedance		ZCIN	1, 7, 13, 69, 75 PIN	135	190	250	kΩ
CYIN input impedance		ZCYIN	21, 27, 33, 39 PIN	135	190	250	kΩ
PbIN input impedance		ZPbIN	23, 29, 35, 41 PIN	135	190	250	kΩ
PrIN input impedance		ZPrIN	25, 31, 37, 43 PIN	135	190	250	kΩ
VOUT (61PIN) electrical characteristics							
VOUT voltage gain		GvVOUT	SIN wave: 1V, f=100kHz	–0.3	0.0	0.3	dB
VOUT frequency characteristic		fVOUT	SIN wave: 1V, 10MHz/100kHz	–1.0	0.0	1.5	dB
VOUT input dynamic range		DRVOUT	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V
VOUT crosstalk		CTVOUT	SIN wave: 1V, f=4.43MHz		–65	–55	dB
VOUT3 (51PIN) electrical characteristics							
VOUT3 voltage gain		GvVOUT3	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB
VOUT3 frequency characteristic	with filter	f1VOUT3	SIN wave: 1V, 6.75MHz/100kHz	–1.0	0.0	1.0	dB
		f2VOUT3	SIN wave: 1V, 27MHz/100kHz		–33.0	–24.0	dB
VOUT3 input dynamic range		DRVOUT3	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V
VOUT3 group delay	with filter	tGDVOUT3	at 100kHz		50		ns
VOUT3 group delay deviation 1	with filter	⊿t1GDVOUT3	to 3.58MHz		4	20	ns
VOUT3 group delay deviation 2	with filter	⊿t2GDVOUT3	to 4.43MHz		7	20	ns
VOUT3 group delay deviation 3	with filter	⊿t3GDVOUT3	to 6MHz		12	20	ns
VOUT3 crosstalk		CTVOUT3	SIN wave: 1V, f=4.43MHz		–65	–55	dB
VOUT4 (48PIN) electrical characteristics							
VOUT4 voltage gain	0dB	Gv1VOUT4	SIN wave: 1V, f=100kHz	–0.3	0.0	0.3	dB
	6dB	Gv2VOUT4	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB
VOUT4 frequency characteristic		fVOUT4	SIN wave: 1V, 10MHz/100kHz	–1.0	0.0	1.0	dB
VOUT4 input dynamic range		DRVOUT4	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V
VOUT4 crosstalk		CTVOUT4	SIN wave: 1V, f=4.43MHz		–65	–55	dB
YOUT3 (52PIN) electrical characteristics							
YOUT3 voltage gain		GvYOUT3	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB
YOUT3 frequency characteristic	with filter	f1YOUT3	SIN wave: 1V, 6.75MHz/100kHz	–1.0	0.0	1.0	dB
		f2YOUT3	SIN wave: 1V, 27MHz/100kHz		–33.0	–24.0	dB
YOUT3 input dynamic range		DRYOUT3	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V
YOUT3 group delay	with filter	tGDYOUT3	at 100kHz		50		ns
YOUT3 group delay deviation 1	with filter	⊿t1GDYOUT3	to 3.58MHz		4	20	ns
YOUT3 Group delay deviation 2	with filter	⊿t2GDYOUT3	to 4.43MHz		7	20	ns
YOUT3 group delay deviation 3	with filter	⊿t3GDYOUT3	to 6MHz		12	20	ns
YOUT3 crosstalk		CTYOUT3	SIN wave: 1V, f=4.43MHz		–45	–43	dB

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
(50PIN) electrical characteristics							
COUT3 voltage gain		GvCOUT3	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB
COUT3 frequency characteristic	with filter	f1COUT3	SIN wave: 1V, 6.75MHz/100kHz	–1.0	0.0	1.0	dB
		f2COUT3	SIN wave: 1V, 27MHz/100kHz		–33.0	–24.0	dB
COUT3 input dynamic range		DRCOUT3	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V
COUT3 group delay	with filter	tGDCOUT3	at 100kHz		50		ns
COUT3 group delay deviation 1	with filter	⊿t1GDCOUT3	to 3.58MHz		4	20	ns
COUT3 group delay deviation 2	with filter	⊿t2GDCOUT3	to 4.43MHz		7	20	ns
COUT3 group delay deviation 3	with filter	⊿t3GDCOUT3	to 6MHz		12	20	ns
COUT3 crosstalk		CTCOUT3	SIN wave: 1V, f=4.43MHz		–45	–43	dB
CYOUT (56,60PIN) electrical characteristics							
CYOUT voltage gain	0dB	Gv1CYOUT	SIN wave: 1V, f=100kHz	–0.3	0.0	0.3	dB
	6dB	Gv2CYOUT	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB
CYOUT frequency characteristic	without filter	f1CYOUT	SIN wave: 1V, 50MHz/100kHz	–3.0	2.0	3.0	dB
	with filter	f2CYOUT	SIN wave: 1V, 13.5MHz/100kHz	–1.0	0.0	1.0	dB
		f3CYOUT	SIN wave: 1V, 54MHz/100kHz		–33.0	–24.0	dB
CYOUT input dynamic range		DRCYOUT	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V
CYOUT group delay	with filter	tGDCYOUT	at 100kHz		25		ns
CYOUT group delay deviation 1	with filter	⊿t1GDCYOUT	to 3.58MHz		1	20	ns
CYOUT group delay deviation 2	with filter	⊿t2GDCYOUT	to 4.43MHz		1	20	ns
CYOUT group delay deviation 3	with filter	⊿t3GDCYOUT	to 12MHz		9	20	ns
CYOUT crosstalk		CTCYOUT	SIN wave: 1V, f=4.43MHz		–65	–55	dB
PbOUT (55,59PIN) electrical characteristics							
PbOUT Voltage gain	0dB	Gv1PbOUT	SIN wave: 1V, f=100kHz	–0.3	0.0	0.3	dB
	6dB	Gv2PbOUT	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB
PbOUT frequency characteristic	without filter	f1PbOUT	SIN wave: 1V, 25MHz/100kHz	–3.0	4.0	5.0	dB
	with filter	f2PbOUT	SIN wave: 1V, 13.5MHz/100kHz	–1.0	2.0	3.0	dB
		f3PbOUT	SIN wave: 1V, 54MHz/100kHz		–33.0	–24.0	dB
PbOUT input dynamic range		DRPbOUT	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V
PbOUT group delay	with filter	tGDPbOUT	at 100kHz		25		ns
PbOUT group delay deviation 1	with filter	⊿t1GDPbOUT	to 3.58MHz		1	20	ns
PbOUT group delay deviation 2	with filter	⊿t2GDPbOUT	to 4.43MHz		1	20	ns
PbOUT group delay deviation 3	with filter	⊿t3GDPbOUT	to 12MHz		9	20	ns
PbOUT crosstalk		CTPbOUT	SIN wave: 1V, f=4.43MHz		–65	–55	dB

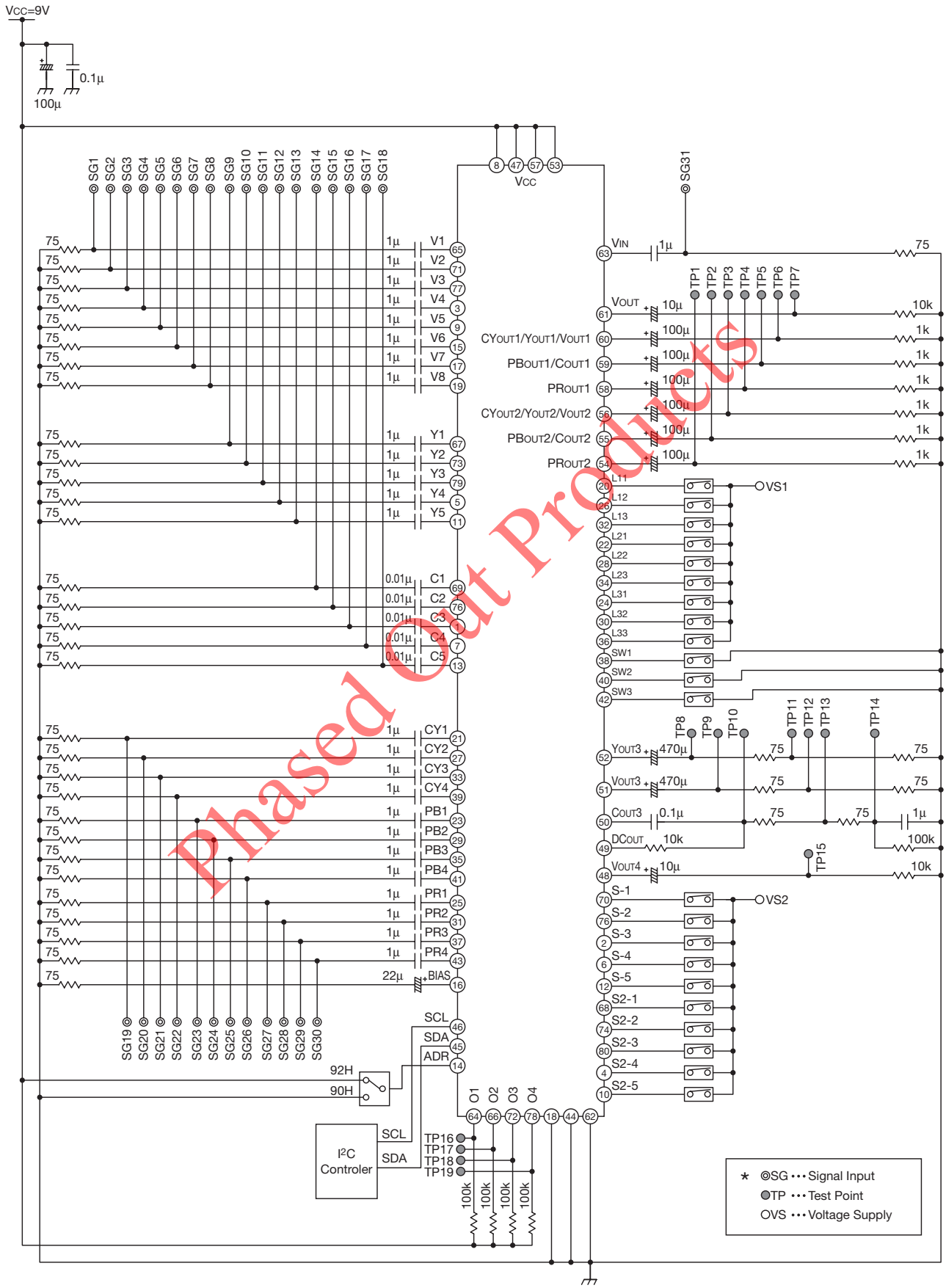
Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
PROUT (54,58PIN) electrical characteristics							
PROUT voltage gain	0dB	$Gv1_{PrOUT}$	SIN wave: 1V, f=100kHz	–0.3	0.0	0.3	dB
	6dB	$Gv2_{PrOUT}$	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB
PROUT frequency characteristic	without filter	$f1_{PrOUT}$	SIN wave: 1V, 25MHz/100kHz	–3.0	4.0	5.0	dB
	with filter	$f2_{PrOUT}$	SIN wave: 1V, 13.5MHz/100kHz	–1.0	2.0	3.0	dB
		$f3_{PrOUT}$	SIN wave: 1V, 54MHz/100kHz		–33.0	–24.0	dB
PROUT input dynamic range		DR_{PrOUT}	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V
PROUT group delay	with filter	$t_{GDPrOUT}$	at 100kHz		25		ns
PROUT group delay deviation 1	with filter	$\Delta t1_{GDPrOUT}$	to 3.58MHz		1	20	ns
PROUT group delay deviation 2	with filter	$\Delta t2_{GDPrOUT}$	to 4.43MHz		1	20	ns
PROUT group delay deviation 3	with filter	$\Delta t3_{GDPrOUT}$	to 12MHz		9	20	ns
PROUT crosstalk		CT_{PrOUT}	SIN wave: 1V, f=4.43MHz		–65	–55	dB
Group delay deviation-between each channels							
Group delay deviation between C and Y		$\Delta t1_{chGD}$	between C and Y at 3.58MHz		0	10	ns
Group delay deviation between CY and Pb (Pr)		$\Delta t2_{chGD}$	between CY and Pb (Pr) at 2MHz		0	10	ns
O1 (64PIN) electrical characteristics							
O1 pin low level output voltage		V_{O1}	O1 PIN sink 1mA	0.0		0.4	V
O1 pin Leak current (at the time of OFF)		I_{O1}		–1.0		1.0	µA
O2 (66PIN) electrical characteristics							
O2 pin low level output voltage		V_{O2}	O2 PIN sink 1mA	0.0		0.4	V
O2 pin Leak current (at the time of OFF)		I_{O2}		–1.0		1.0	µA
O3 (72PIN) electrical characteristics							
O3 pin low level output voltage		V_{O3}	O3 PIN sink 1mA	0.0		0.4	V
O3 pin Leak current (at the time of OFF)		I_{O3}		–1.0		1.0	µA
O4 (78PIN) electrical characteristics							
O4 pin low level output voltage		V_{O4}	O4 PIN sink 1mA	0.0		0.4	V
O4 pin leak current (at the time of OFF)		I_{O4}		–1.0		1.0	µA

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
I²C condition						
Input voltage L	V_{IL}		0.0		0.8	V
Input voltage H	V_{IH}		2.2		5.0	V
SDA low level output voltage	V_{OL}	SDA sink 3mA	0.0		0.4	V
High level input current	I_{IH}	SDA, SCL=4.5V	–10		10	µA
Low level input current	I_{IL}	SDA, SCL=0.4V	–10		10	µA
Clock Frequency	f_{SCL}				100	kHz
Data transfer wait time	t_{BUF}		4.7			µs
SCL start hold time	$t_{HD;STA}$		4.0			µs
SCL low level hold time	t_{LOW}		4.7			µs
SCL high level hold time	t_{HIGH}		4.0			µs
Start condition setup time	$t_{SU;STA}$		4.7			µs
SDA data hold time	$t_{HD;DAT}$		200			ns
SDA data setup time	$t_{SU;DAT}$		250			ns
SDA,SCL rise time	t_R				1000	ns
SDA,SCL fall time	t_F				300	ns
Stop condition setup time	$t_{SU;STO}$		4.0			µs

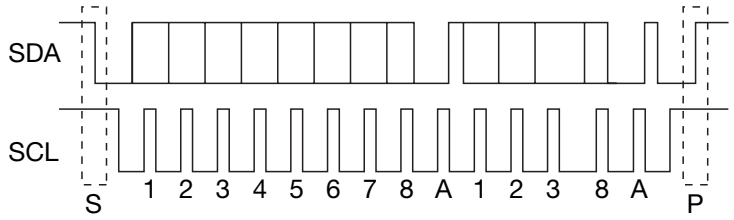
Note I²C condition



Measuring Circuit



I²C BUS

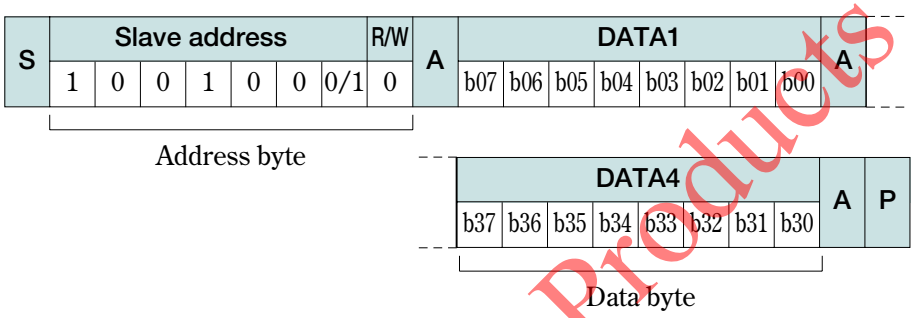


S:Start Condition
P:Stop Condition
A:Acknowledge

I²C BUS is inter bus system controlled by 2 lines (SDA.SCL).
Data are transmitted and received in the units of byte and Acknowledge.
It is transmitted by MSB first from the start conditions.

[Control registers]

Control registers are data sent from the master for determining the switch conditions.
The data format is set as shown in the following figure.)



Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.
Set the R/W bit to 0 when data are used control registers.
As MM1630 slave address, either 90H or 92H can be selected according to the ADR terminal conditions. When ADR terminal is L, 90H is selected.
The following figure indicates the control contents of control registers and switches.
Each bit of control registers is reset to 0, when power-on.

MM1630 consists of one address byte and 4 control data bytes (5bytes in total).
All data over the limited length (XXXth and subsequent bytes) are fully neglected.
For details of the control contents of switches, refer to the another table.

No.	DATA condition							
DATA1 (00H)	b07	b06	b05	b04	b03	b02	b01	b00
	OUT1 LPF SW	OUT1 Power Save	OUT1 GAIN SW	OUT1 LINE SELECT				
DATA2 (00H)	b17	b16	b15	b14	b13	b12	b11	b10
	OUT2 LPF SW	OUT1 Power Save	OUT1 GAIN SW	OUT2 LINE SELECT				
DATA3 (00H)	b27	b26	b25	b24	b23	b22	b21	b20
	OUT4 LINE SELECT				OUT3 LINE SELECT			
DATA4 (00H)	b37	b36	b35	b34	b33	b32	b31	b30
	O4 OUTPUT	O3 OUTPUT	O2 OUTPUT	O1 OUTPUT	DCout OUTPUT VOLTAGE		OUT4 GAIN SW	

* [00H] is in the initial state of control registers.

Switch Control Table

OUT1 LINE SELECT

b04	b03	b02	b01	b00	VOUT1	PBOUT1	PROUT1	VOUT
0	0	0	0	0	Mute	Mute	Mute	Mute
0	0	0	0	1	V1	Mute	Mute	V1
0	0	0	1	0	V2	Mute	Mute	V2
0	0	0	1	1	V3	Mute	Mute	V3
0	0	1	0	0	V4	Mute	Mute	V4
0	0	1	0	1	V5	Mute	Mute	V5
0	0	1	1	0	V6	Mute	Mute	V6
0	0	1	1	1	V7	Mute	Mute	V7
0	1	0	0	0	V8	Mute	Mute	V8
0	1	0	0	1	V1 (GRS)	Mute	Mute	V1
0	1	0	1	0	V2 (GRS)	Mute	Mute	V2
0	1	0	1	1	V3 (GRS)	Mute	Mute	V3
0	1	1	0	0	V4 (GRS)	Mute	Mute	V4
0	1	1	0	1	V5 (GRS)	Mute	Mute	V5
0	1	1	1	0	V6 (GRS)	Mute	Mute	V6
0	1	1	1	1	V7 (GRS)	Mute	Mute	V7
1	0	0	0	0	V8 (GRS)	Mute	Mute	V8
1	0	0	0	1	Y1	C1	Mute	Mute
1	0	0	1	0	Y2	C2	Mute	Mute
1	0	0	1	1	Y3	C3	Mute	Mute
1	0	1	0	0	Y4	C4	Mute	Mute
1	0	1	0	1	Y5	C5	Mute	Mute
1	0	1	1	0	CY1	PB1	PR1	Mute
1	0	1	1	1	CY2	PB2	PR2	Mute
1	1	0	0	0	CY3	PB3	PR3	Mute
1	1	0	0	1	CY4	PB4	PR4	Mute
1	1	0	1	0	Mute	Mute	Mute	Mute
			≀		Mute	Mute	Mute	Mute
1	1	1	1	1	Mute	Mute	Mute	Mute

OUT2 LINE SELECT

b14	b13	b12	b11	b10	VOUT2	PBOUT2	PROUT2
0	0	0	0	0	Mute	Mute	Mute
0	0	0	0	1	V1	Mute	Mute
0	0	0	1	0	V2	Mute	Mute
0	0	0	1	1	V3	Mute	Mute
0	0	1	0	0	V4	Mute	Mute
0	0	1	0	1	V5	Mute	Mute
0	0	1	1	0	V6	Mute	Mute
0	0	1	1	1	V7	Mute	Mute
0	1	0	0	0	V8	Mute	Mute
0	1	0	0	1	Mute	Mute	Mute
		≀			Mute	Mute	Mute
1	0	0	0	0	Mute	Mute	Mute
1	0	0	0	1	Y1	C1	Mute
1	0	0	1	0	Y2	C2	Mute
1	0	0	1	1	Y3	C3	Mute
1	0	1	0	0	Y4	C4	Mute
1	0	1	0	1	Y5	C5	Mute
1	0	1	1	0	CY1	PB1	PR1
1	0	1	1	1	CY2	PB2	PR2
1	1	0	0	0	CY3	PB3	PR3
1	1	0	0	1	CY4	PB4	PR4
1	1	0	1	0	Mute	Mute	Mute
		≀			Mute	Mute	Mute
1	1	1	1	1	Mute	Mute	Mute

OUT3 LINE SELECT

b23	b22	b21	b20	VOUT3	YOUT3	COUT3
0	0	0	0	Mute	Mute	Mute
0	0	0	1	Y1+C1	Y1	C1
0	0	1	0	Y2+C2	Y2	C2
0	0	1	1	Y3+C3	Y3	C3
0	1	0	0	Y4+C4	Y4	C4
0	1	0	1	Y5+C5	Y5	C5
0	1	1	0	V1	Mute	Mute
0	1	1	1	V2	Mute	Mute
1	0	0	0	V3	Mute	Mute
1	0	0	1	V4	Mute	Mute
1	0	1	0	V5	Mute	Mute
1	0	1	1	V6	Mute	Mute
1	1	0	0	V7	Mute	Mute
1	1	0	1	V8	Mute	Mute
1	1	1	0	CY4+PB4	CY4	PB4
1	1	1	1	Mute	Mute	Mute

OUT4 LINE SELECT

b27	b26	b25	b24	VOUT4
0	0	0	0	Mute
0	0	0	1	Y1+C1
0	0	1	0	Y2+C2
0	0	1	1	Y3+C3
0	1	0	0	Y4+C4
0	1	0	1	Y5+C5
0	1	1	0	V1
0	1	1	1	V2
1	0	0	0	V3
1	0	0	1	V4
1	0	1	0	V5
1	0	1	1	V6
1	1	0	0	V7
1	1	0	1	V8
1	1	1	0	CY4+PB4
1	1	1	1	Mute

DCOUT OUTPUT VOLTAGE

b33	b32	DCOUT
0	0	0V
0	1	2.2V
1	*	5V

GAIN SW

bit	GAIN
0	0dB
1	6dB

Power save SW

bit	Conditions
0	Active
1	Power Save

LPF SW

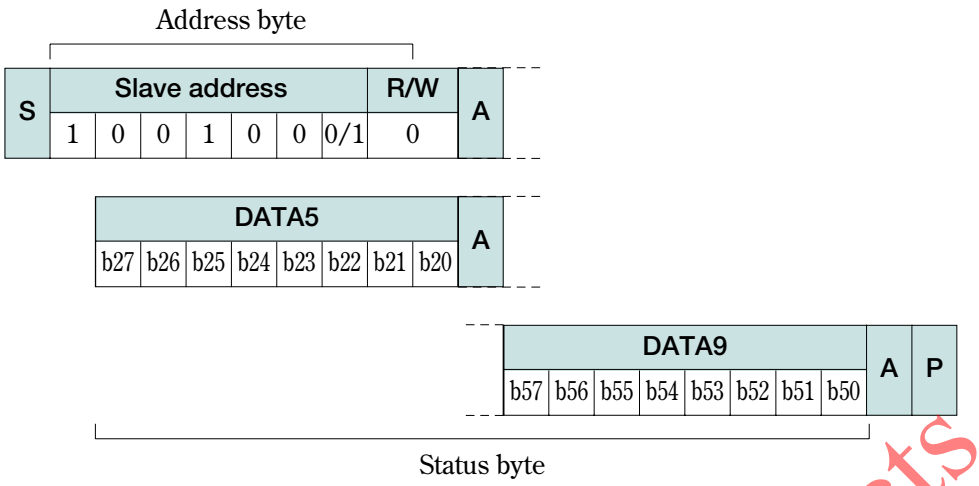
bit	LPF
0	without filter
1	with filter

O1~O4 OUTPUT

bit	O1~O4
0	Low
1	Open

[Status registers]

Status registers are data to inform the master of the device status.
The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address,while the residual 1bit is assigned to the R/W bit. Set the R/W bit to 1 when data are used status registers.
As MM1630 slave address, either 91H or 93H can be selected according to the ADR terminal conditions. When ADR terminal is L, 91H is selected.
Set the confirmation acknowledgement after the end of status register to non-ACK.
The following figure shows the correspondence of the output data of status registers.

No.	DATA condition							
DATA5	b47	b46	b45	b44	b43	b42	b41	b40
	L31 DETECT		L13 DETECT		L12 DETECT		L11 DETECT	
DATA6	b57	b56	b55	b54	b53	b52	b51	b50
	SW1 DETECT	L23 DETECT	L22 DETECT	L21 DETECT	L33 DETECT		L32 DETECT	
DATA7	b67	b66	b65	b64	b63	b62	b61	b60
	S2–3 DETECT		S2–2 DETECT		S2–1 DETECT		SW3 DETECT	SW2 DETECT
DATA8	b77	b76	b75	b74	b73	b72	b71	b70
	S4 DETECT	S3 DETECT	S2 DETECT	S1 DETECT	S2–5 DETECT		S2–4 DETECT	
DATA9	b87	b86	b85	b84	b83	b82	b81	b80
	1							S5 DETECT

L11, L12, L13 DETECT (Scanning Line)

L11~L13 Voltage	Scanning Line	2bit	1bit
DC ≦ 1.0V	480	0	0
1.3V ≦ DC ≦ 2.7V	720	0	1
3.5V ≦ DC ≦ 5.0V	1080	1	0

S2-1~S2-5 DETECT (Aspect)

S2-1~S2-5 Voltage	Aspect	2bit	1bit
DC ≦ 1.0V	4 : 3	0	0
1.3V ≦ DC ≦ 2.7V	Letter box	0	1
3.5V ≦ DC ≦ 5.0V	16 : 9	1	0

L21, L22, L23 DETECT (IP)

L21~L23 Voltage	I/P	1bit
DC ≦ 2.7V	Interlace	0
3.5V ≦ DC ≦ 50V	Progressive	1

S1~S5 DETECT

S1~S5 Voltage	Conditions	bit
DC ≦ 4.2V	CONNECTED	1
5.3V ≦ DC	UNCONNECTED	0

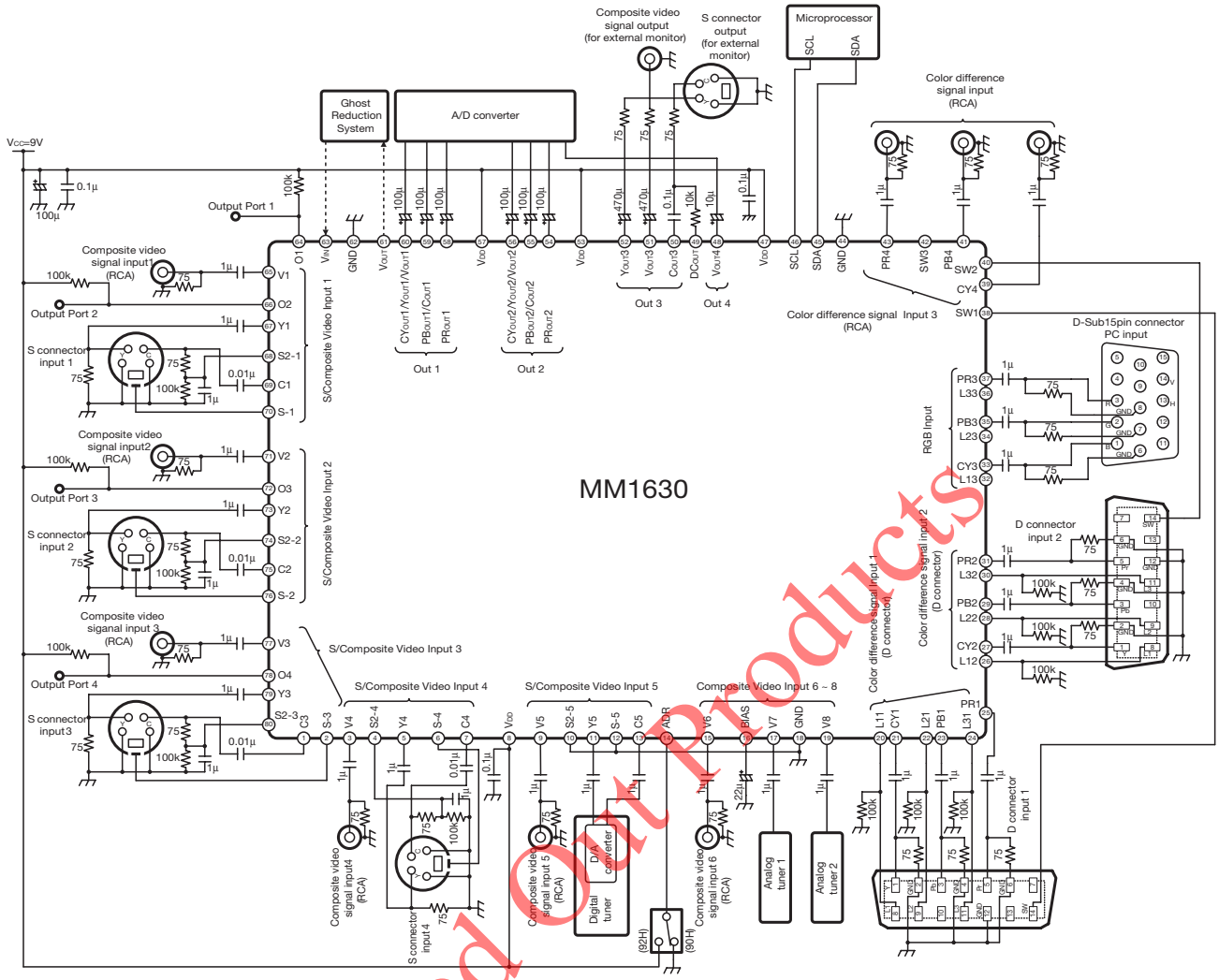
L31, L32, L33 DETECT (Aspect)

L31~L33 Voltage	Aspect	2bit	1bit
DC ≦ 1.0V	4 : 3	0	0
1.3V ≦ DC ≦ .7V	Letter box	0	1
3.5V ≦ DC ≦ 5.0V	16 : 9	1	0

SW1~SW3 DETECT

SW1~SW3 Voltage	Conditions	bit
DC ≦ 4.2V	CONNECTED	1
5.3V ≦ DC	UNCONNECTED	0

Application Circuit



Note:

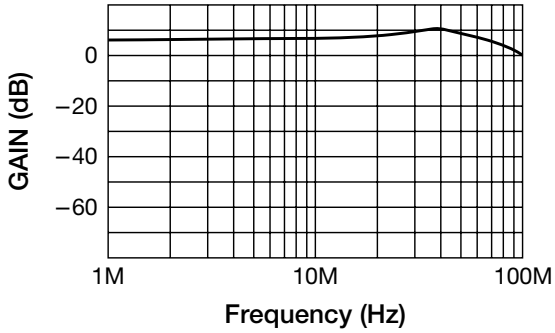
·We shall not be liable for any trouble or damage caused by using this circuit.

·In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, we shall not be liable for any such problem, nor grant a license therefore.

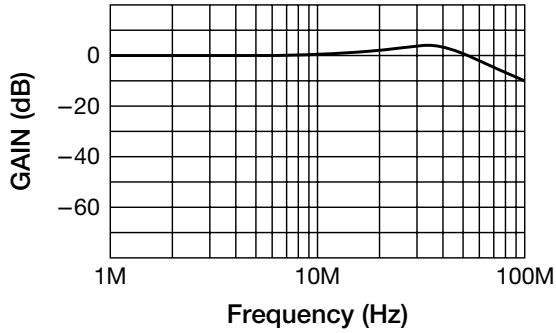
Characteristics (Except where noted otherwise, Ta=25°C, Vcc=9V)

A. Frequency Characteristics

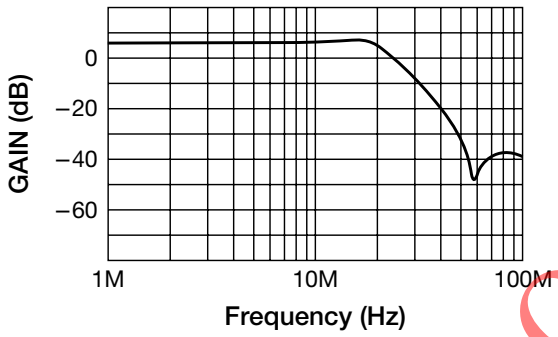
■ CYOUT1, 2 THRU 6dB



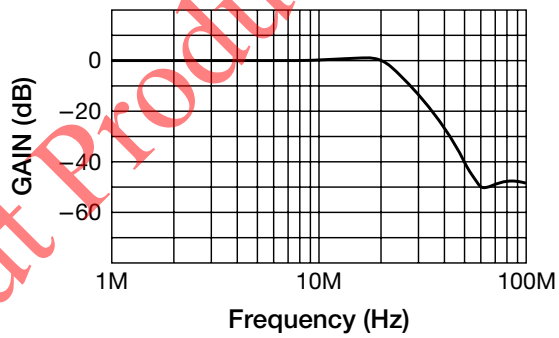
■ CYOUT1, 2 THRU 0dB



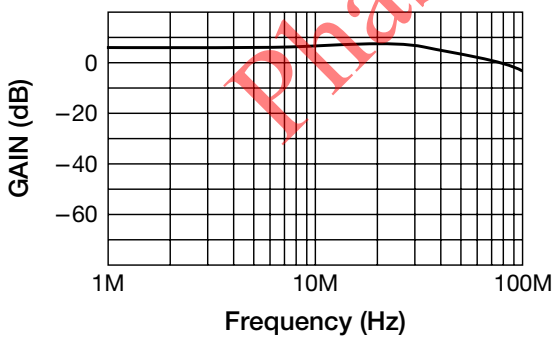
■ CYOUT1, 2 LPF 6dB



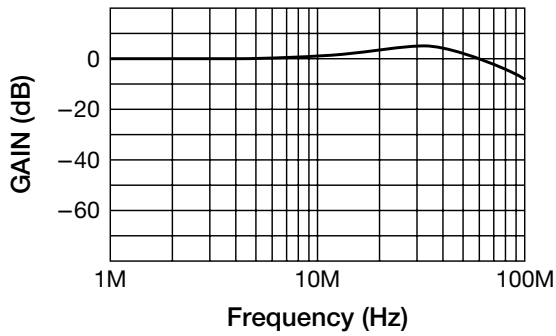
■ CYOUT1, 2 LPF 0dB



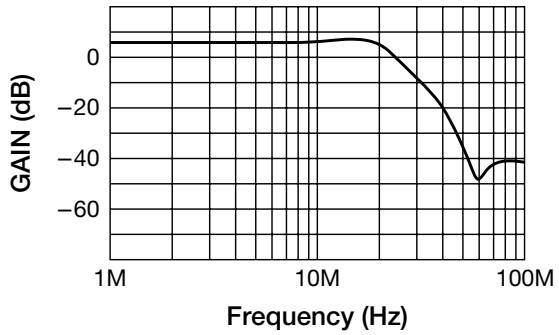
■ Pb, PROUT1, 2 THRU 6dB



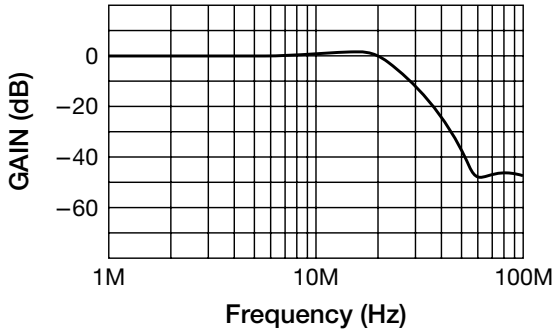
■ Pb, PROUT1, 2 THRU 0dB



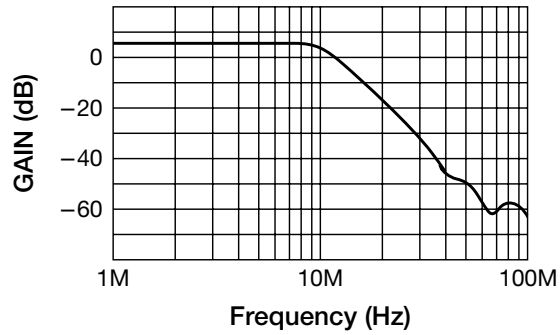
Pb, PROUT1, 2 LPF 6dB



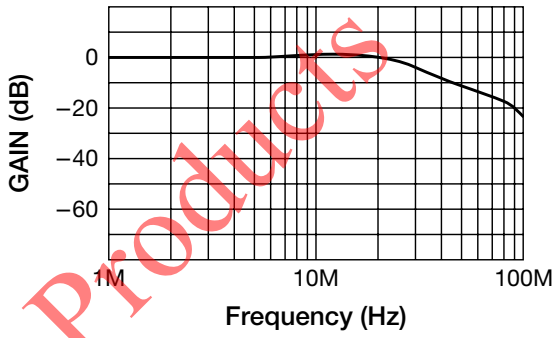
Pb, PROUT1, 2 LPF 0dB



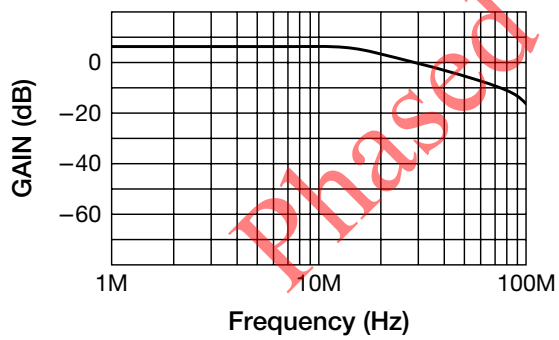
V, Y, COUT3



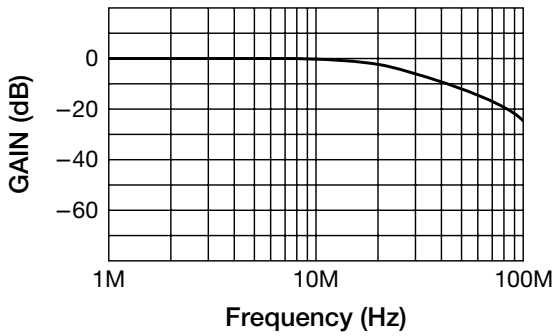
VOUT



VOUT4 6dB

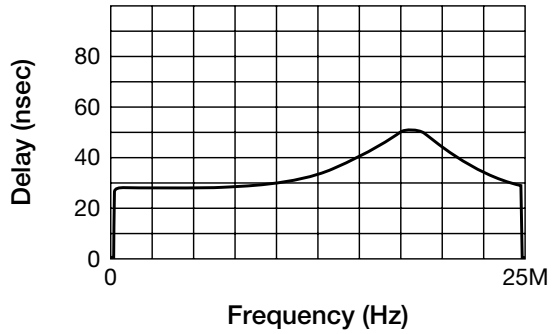


VOUT4 0dB

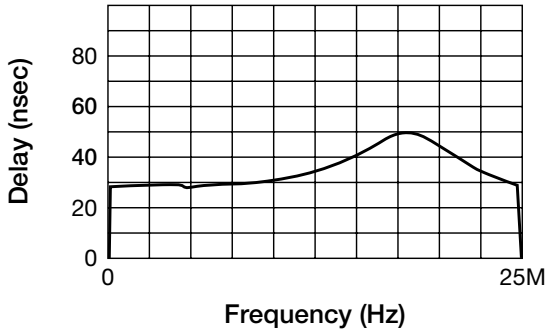


B. Group delay

CYOUT LPF



Pb, PROUT LPF



V, Y, COUT3