IGBT & SiC Gate Driver Fundamentals

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IGBT and SiC power switch fundamentals

Outline

- IGBT and SiC Power Switch Fundamentals
- Isolated Gate Driver Features
- IGBT and SiC Protection Basics

IGBT and SiC power switch fundamentals

- What are the markets and applications for insulated gate bipolar transistors (IGBTs) and silicon carbide (SiC) power switches?
- What are the advantages of SiC metal-oxide semiconductor field-effect transistors (MOSFETs) over IGBTs and silicon (Si) MOSFET power switches?
- What are the differences between Si MOSFET, IGBT and SiC power switches?

IGBT and SiC applications

What are the markets and applications for IGBT and SiC power switches?

Efficient power conversion is heavily dependent on the power semiconductor devices used in the system. High-power applications are becoming more efficient and smaller in size because of improvements in power device technology. Such devices include IGBTs and SiC MOSFETs, which are a good fit in high-power applications due to their high voltage ratings, high current ratings, and low conduction and switching losses.

Specifically, applications with bus voltages >400 V require device voltage ratings >650 V to leave sufficient margin for safe operation. Applications including industrial motor drives, electric vehicles/ hybrid electric vehicles (EVs/HEVs), traction inverters and solar inverters for renewable energy are at the power level of a few kilowatts (kW) to a megawatt (MW) and beyond. Applications for SiC MOSFETs and IGBTs are at similar power levels, but split as the frequency increases, as shown in **Figure 1**.

SiC MOSFETs are becoming common in power factor correction power supplies, solar inverters, DC/DC for EVs/HEVs, traction inverters for EVs, motor drives and railway, while IGBTs are common in motor drives (AC machines), uninterruptible power supplies (UPSs), solar central- and string-type power inverters <3 kW, and traction inverters EVs/HEVs.

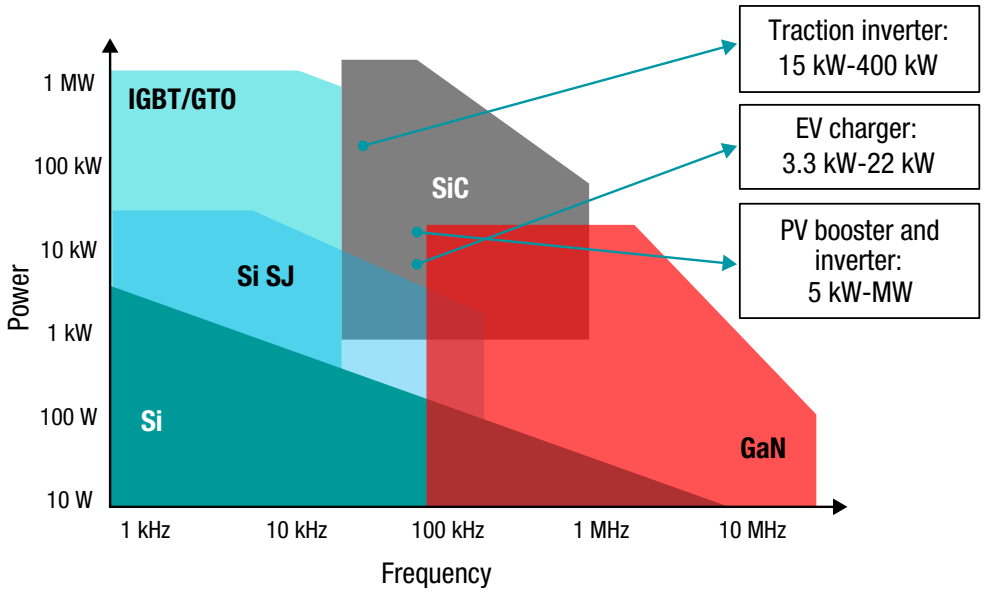


Figure 1: *Power semiconductor device applications based on power and frequency levels*

IGBT and SiC applications

What are the system advantages of SiC MOSFETs over silicon (Si) MOSFETs and IGBTs?

Si MOSFETs and IGBTs have been used in power converters for a long time. However, SiC MOSFETs have emerged as a new technology, showing benefits surpassing those devices given their intrinsic material properties: a wide-bandgap (WBG) material. These characteristics are summarized in **Table 1**. The material properties of SiC directly translate into system-level advantages over systems using Si devices, including reduced size, cost and weight. Consequently, SiC MOSFETs are increasingly replacing Si power devices.

Property	Definition	Si	SiC – 4H
E_G (eV)	Bandgap energy	1.12	3.26
E_{BR} (MV/cm)	Critical field breakdown voltage	0.3	3.0
V_S (x10^7 cm/s)	Saturation velocity	1.0	2.2
μ (cm^2/V*s)	Electron Mobility	1400	900
^ (W/cm*K)	Thermal conductivity	1.3	3.7

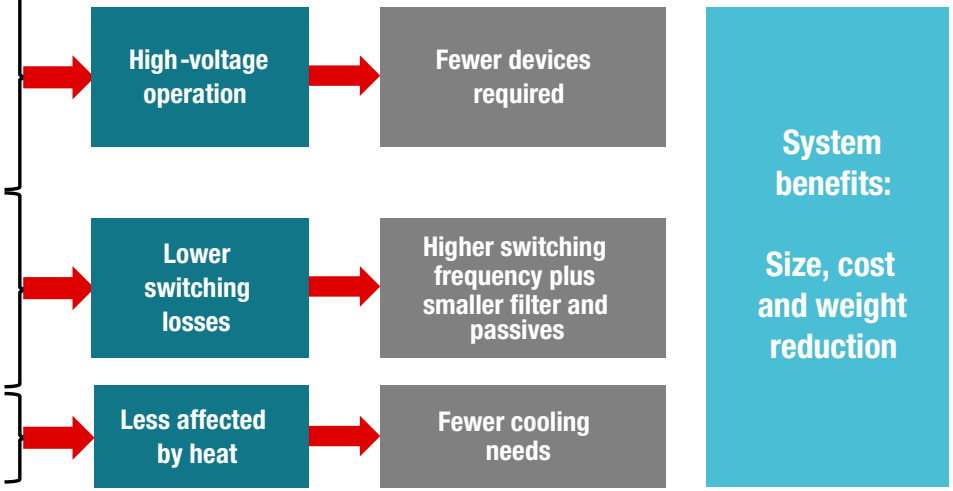


Table 1: *Power device material characteristics*

IGBT and SiC power switch fundamentals

What are the differences between Si MOSFET, Si IGBT and SiC MOSFET power switches?

Si MOSFETs, Si IGBTs and SiC MOSFETs are all used in power applications but vary with regards to their power levels, drive methods and operating modes. Both power IGBTs and MOSFETs are voltage-driven at the gate, since the IGBT is internally a MOSFET driving a bipolar junction transistor (BJT). Due to the bipolar nature of IGBTs, they carry a large amount of current with a low saturation voltage, resulting in low conduction losses. MOSFETs have low conduction losses as well, but depend on the device's drain-to-source on-resistance, $R_{DS(ON)}$, versus an on-state voltage. Si MOSFETs carry less current than IGBTs, so IGBTs are used in high-power applications. MOSFETs are used in high-frequency applications where high efficiency is key.

SiC MOSFETs are similar to Si MOSFETs with respect to the device type. However, SiC is a WBG material with properties that allow these devices to operate at the same high power levels as IGBTs while still being able to switch at high frequencies. These properties translate into system benefits including higher power density, higher efficiency and lower heat dissipation.

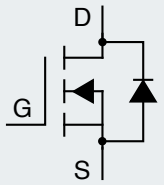
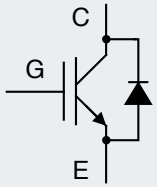
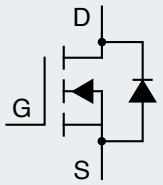
	Si MOSFETs	Si IGBTs	SiC MOSFETs
Circuit symbol			
Voltage rating	20 V-650 V	≥650 V	≥650 V
f_{sw}	Medium-high (>20 kHz)	Low-medium (5 kHz-20 kHz)	High (>50 kHz)
V_{GS}/V_{GE}	0 V-15 V (20 V)	-10 V-15 V (10 V-20 V)	-5 V-20 V (25 V-30V)
Typical applications	Power supplies – server, telecom, factory automation, offboard/onboard chargers, solar inverters, string inverters	Motor drives (AC machines), UPSs, solar central and string power inverters, EV/HEV traction inverters	PFC – power supplies, solar inverters, DC/DC for EVs/HEVs, traction inverters for EVs, motor drives, railways
Power level	<3 kW	>3 kW	>5 kW

Table 2: *Power device ratings and applications*

Isolated gate driver features

- What are some common forms of isolation and how do they differ?
- Why is isolation required for high-voltage applications?
- How is the drive strength determined for a power switch?
- Why are split outputs better than a single output for driving a power switch?
- Why is high drive strength beneficial for IGBTs and SiC MOSFETs?
- Why is it critical to maintain a minimum dead time for power system operation?
- Why is low propagation delay critical for high-frequency power systems?
- Why is it critical to have tight part-to-part propagation delay matching?
- Why is high undervoltage lockout (UVLO) important for safe IGBT and SiC MOSFET power switch operation?
- What is an input deglitch filter, and why are they important in high-power applications?
- What is interlock protection, and how is it implemented in a driver?
- Why is temperature sensed in a power converter?
- What is common-mode transient immunity (CMTI), and how is it measured?
- Why is isolated sensing important, and how accurate does it need to be?

Isolation technology

What are some common forms of isolation, and how do they differ?

Isolation is important for system reliability and human safety. Various forms of electrical isolation are available. The three main types are optical, magnetic and capacitive. Each type uses a different methodology to transfer an AC or DC signal to the output reliably and without an actual electrical connection. Optical isolation, as shown in **Figure 2**, transmits a signal by driving an LED light. The LED is located close to a phototransistor, which turns the light signal into a current buffered by a complementary metal-oxide semiconductor (CMOS) circuit. Magnetic isolation, shown in **Figure 3,** uses a transformer's windings to transmit signals across an air gap through a magnetic field. The magnetic field at the input induces a current through the output proportional to the original signal. Capacitive isolation, shown in **Figure 4**, uses the electric field to transmit signals between two conductive plates.

Isolation type	Current draw	Reliability	Noise immunity
Optical	High	Medium	Low
Magnetic	High	Medium	Low
Capacitive	Low	High	High

Table 3: *Types of isolation*

The main considerations when choosing the right kind of isolation barrier are the isolation level, CMTI rating, and degradation and lifetime.

The working voltage of Texas Instruments' (TI) capacitive isolation technology is determined by the time dependent dielectric breakdown (TDDB), which considers all degredation mechanisms. TI's capacitive technology shows the ability to handle much higher stress voltages as compared to optocoupler-based and transformer-based isolation.

TI white papers on isolation

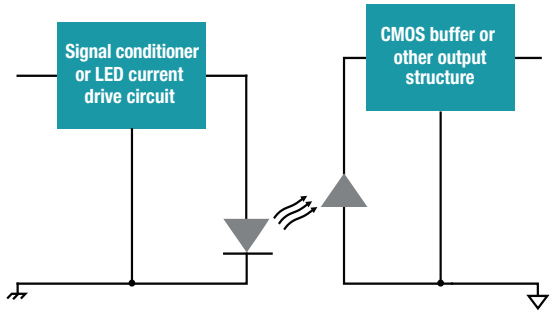


Figure 2: *Optical isolation*

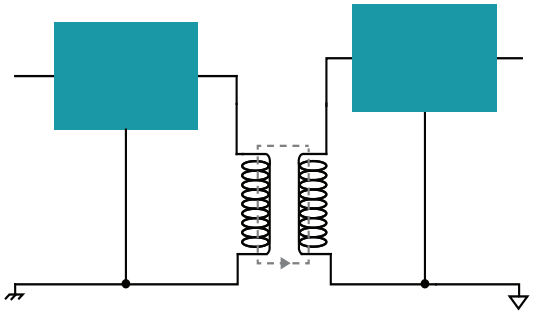


Figure 3: *Magnetic isolation*

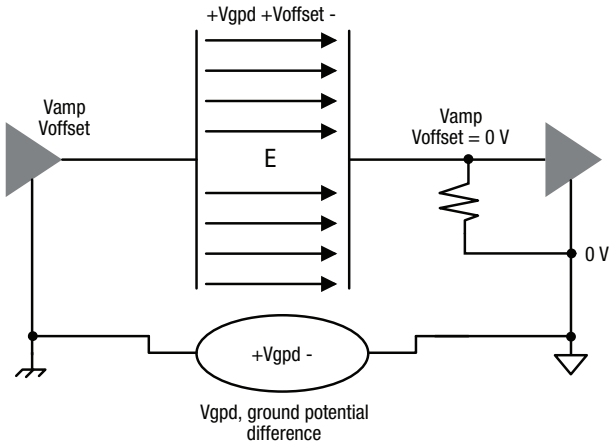


Figure 4: *Capacitive isolation*

Isolation technology

Why is isolation required for high-voltage applications?

Many systems comprise both low- and high-voltage circuits. These circuits are interconnected to combine all of the functions of control and power. For example, the block diagram of a traction inverter is shown in **Figure 5**. This includes the low-voltage communication, control and main power supply circuitry on the primary side. On the secondary side are the high-voltage circuits, including the motor drive, power stage and other auxiliary circuits. The controller uses feedback signals from the high-voltage side, and is susceptible to high voltage and consequently damage if no isolation barrier is present.

An isolation barrier electrically isolates circuitry from the primary to the secondary side by forming separate ground references, also called galvanic isolation. This prevents unwanted AC or DC signals from traveling from one side to the other. The primary side will not exceed the circuitry's maximum ratings. Additionally, the control circuitry may be accessible by humans, and thus high-voltage isolation is necessary to prevent electric shock.

There are three main types of isolation: functional, basic and reinforced. Functional isolation refers to the level of isolation to ensure proper operation, but not to protect against shock. Basic isolation provides sufficient protection against electric shock as long as the isolation barrier remains intact. Guidelines for safety require the use of reinforced isolation, which is double the basic isolation level, to provide redundancy.

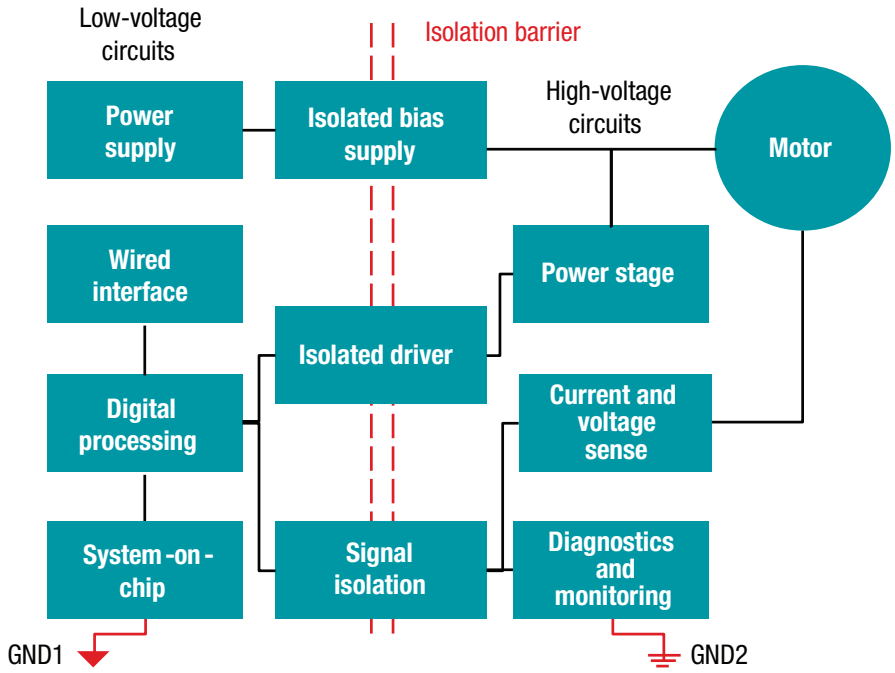


Table 5: *Traction inverter block diagram*

Basic gate driver features

How is the drive strength determined for a power switch?

The drive strength refers to the gate driver's current source and sink capability. Choosing the drive strength depends on the power switch used (IGBT or MOSFET), based on its gate charge. The gate charge is the required amount of charge, or the current in a given period of time, in order to charge and discharge the input capacitance, $C_{ISS} = C_{gd} + C_{gs}$, as shown in **Figure 6**. Gate charge is given as the integral of gate current over a period of time and is rearranged to solve for the required gate current:

$$Q_G = \int I_G dt \rightarrow I_G = \frac{Q_G}{t_{rise/fall}}$$

where $t_{rise/fall}$ is the desired rise and fall time of the gate voltage to increase the switching speed. Gate charge is given in most data sheets as a plot like the one shown in **Figure 7**, describing the regions where the charge is distributed to C_{gd} or C_{gs}. The most critical region is the Miller plateau region, where C_{gd} is charged and the gate voltage is constant. During this region, the voltage switched across the device changes states and results in switching loss. Thus, the driver should be capable of providing the maximum drive strength during this region. The power required of the gate driver is given by:

$$P_{sw} = V_{DRV} * Q_G * f_{sw}$$

where f_{sw} is the switching frequency and V_{DRV} is the drive voltage.

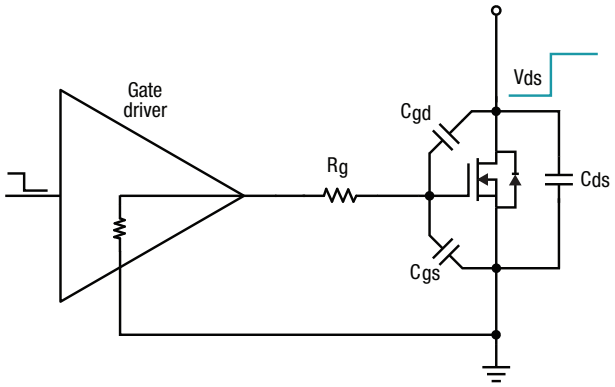


Figure 6: *Power device input capacitance*

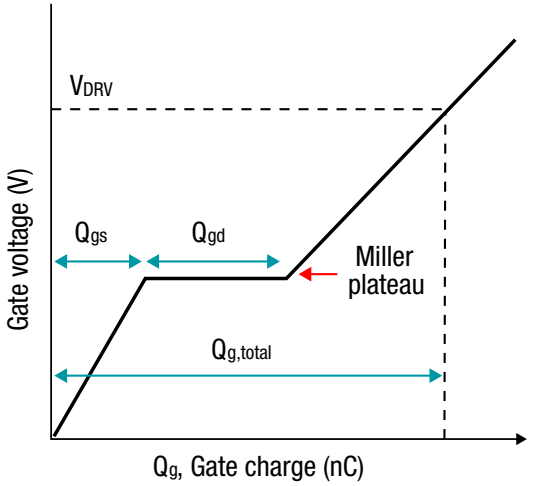


Figure 7: *Power device gate charge plot*

Basic gate driver features

Why are split outputs better than a single output for driving a power switch?

The gate driver sources and sinks current at the gate of a power-switching device to turn it on and off. The speed of the switching power device is dependent on the drive current. To calculate the drive current available from the driver, use the applied gate drive voltage and gate resistance:

$$I_G = V_{OUT}/R_G$$

Gate resistors control the speed of the transient voltage (dv/dt) and transient current (di/dt) of the device, to limit noise from switching and switching losses. For power devices, rise time, fall time, and delays between turnon and turnoff are usually different, and thus require separate consideration. For example, the di/dt at turnoff can result in a large voltage overshoot, so it is beneficial to reduce the switching speed. However, during turnon it is better to switch fast, in order to reduce switching losses.

Gate drivers can have either single or split outputs. **Figure 8** shows a single-output driver. In this case, a diode separates the control for turnon and turnoff. This increases bill-of-materials cost, takes up more space on the gate driver board and adds impedance in the gate loop. As an alternative, a split output driver has separate turnon and turnoff paths for complete and separate control over the drive source or sink strength. Having lower R_G at turnoff is beneficial for SiC MOSFETs to prevent false turnon caused by fast switching and Miller current. Thus, split outputs (**Figure 9**) are the best option to control the power device efficiently and safely.

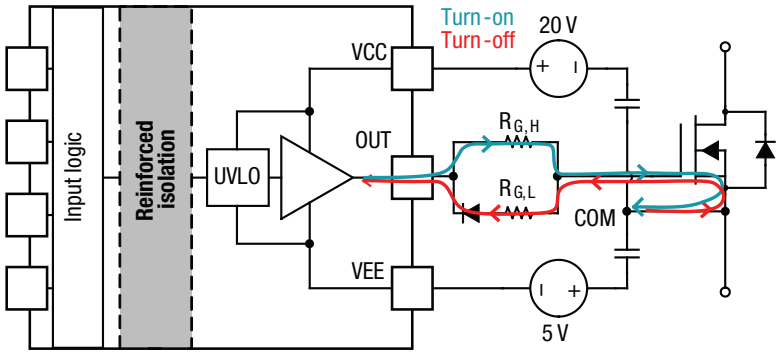


Figure 8: *Driver with a single output*

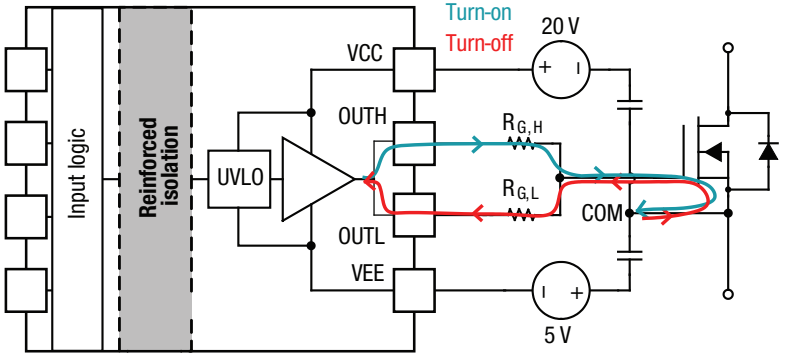


Figure 9: *Driver with split outputs*

Basic gate driver features

Why is high drive strength beneficial for IGBTs and SiC MOSFETs?

IGBTs and SiC MOSFETs have losses during switching transients as the voltage and current overlap, as shown in **Figure 10**. The gate current, or drive strength, determines how fast the device's input capacitors charge and discharge, denoted as t_{sw} in the figure. As gate current increases, t_{sw} decreases. If the current is too small, the losses will increase. The required gate-drive strength depends on the gate charge of the device, Q_G, as shown in **Figure 11**. The average current required to charge the device from when V_{gs} increases past V_{th} to the maximum drive voltage, V_{DRV}, in a time of t_{on} is calculated as:

$$I_G = \frac{Q_G}{t_{on}}$$

This current is the average current required to turn the device fully on. The region of interest, however, is the Miller plateau region, where the gate voltage is constant during the switching transient. The gate driver must be able to supply maximum current during this region to reduce switching losses. This is dependent on the gate resistor and drive voltage during that plateau. SiC MOSFETs can switch very fast, lending themselves to high-power and high-frequency applications. The gate current must be high for the device to provide these benefits. Faster switching results in minimized passive components, and thus overall system size and weight. Both IGBTs and SiC MOSFETs provide system-level benefits when switching fast and efficiently.

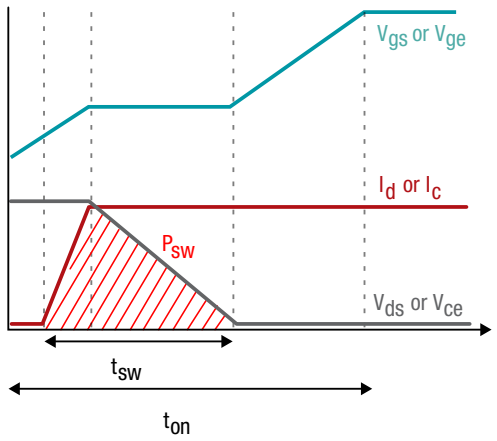


Figure 10: *Device turn-on switching losses*

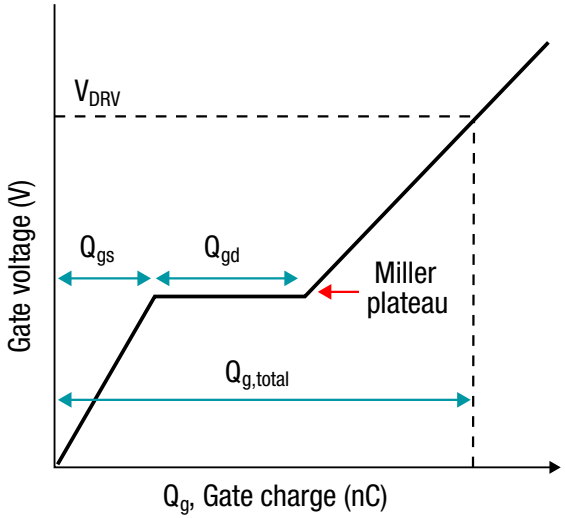


Figure 11: *Device gate charge plot*

Basic gate driver features

Why is it critical to maintain a minimum dead time for power system operation?

Dead time is critical in many switch-mode power converters, inverters and motor drives. The dead time is the period during which neither device is switched to avoid any potential overlap when they are in a half-bridge configuration, as shown in **Figure 12**. There are a few factors that affect the dead-time setting: the pulse-width distortion, propagation delay, and rise and fall times. The pulse-width distortion is determined by the propagation delay mismatch of the rising and falling edges, as shown in **Figure 13**. The propagation delay is also critical, especially when two separate drivers are used for the high and low sides. There can be mismatch between the two, as shown in **Figure 14**. Additionally, rise and fall times may also affect the overlap of these signals. The largest of these parameters is the minimum allowable dead time, plus some margin of error.

In power systems, it is critical to maintain a minimum dead time in order to improve converter efficiency. During the dead time, current flows back through the IGBT or MOSFET body diode, as shown in **Figure 12**. The body diode has a much larger voltage drop than the device itself, and thus there are more conduction losses. The longer the dead time, the higher the losses, which reduce efficiency and generate heat. Thus, it is best to minimize the dead time by using a gate driver with low pulse-width distortion, low propagation delay, and small rise and fall times.

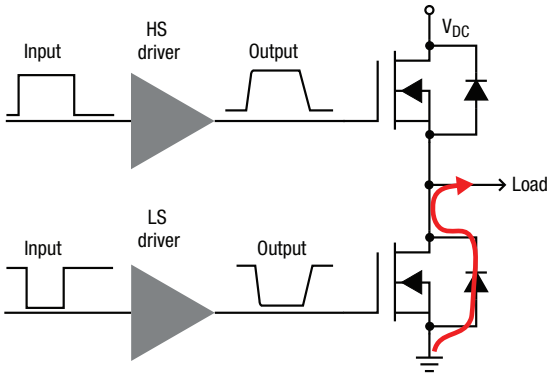


Figure 12: *Synchronously switched half bridge*

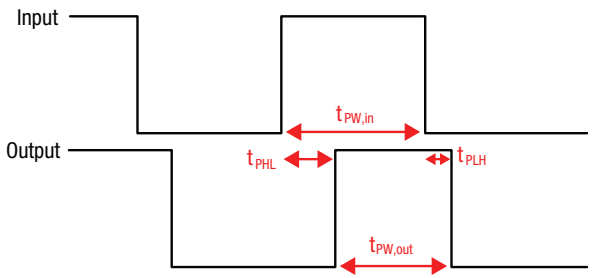


Figure 13: *Pulse-width distortion*

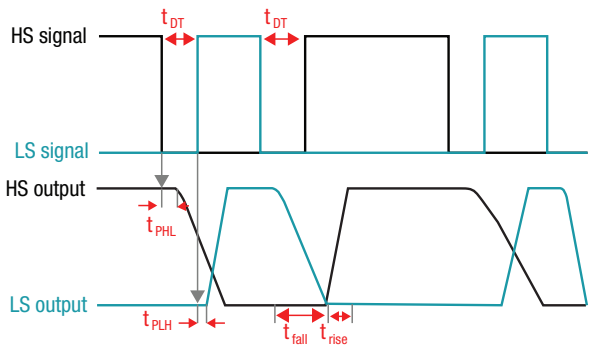


Figure 14: *Effects of propagation delay mismatch*

Basic gate driver features

Why is low propagation delay critical for high-frequency power systems?

High-frequency power systems are now possible due to WBG devices like SiC MOSFETs. In these systems, higher frequency enables higher power density by minimizing filtering components, thereby minimizing the system. Higher frequency also means higher switching losses, however. Thus, it is crucial to minimize losses. Propagation delay is one of the key parameters of a gate driver that can affect the losses and safety of high-frequency systems. Propagation delay is defined as the time delay from 50% of the input to 50% of the output, as shown in **Figure 15**. This delay affects the timing of the switching between devices, which is critical in high-frequency applications where the dead time, or off time between devices, is limited. Dead time is necessary so that two devices do not turn on at the same time, which would cause shoot-through and reduced efficiency. If the dead time is smaller than the propagation delay, then both devices will turn on at the same time, as shown in **Figure 16**.

Making the dead time larger than the propagation delay, however, results in reduced system efficiency. This result is critical when using SiC MOSFETs because current can flow back through the body diode during the dead time. The voltage drop across this diode is large, and thus increases losses. Other applications where propagation delay is critical include paralleling MOSFETs and IGBTs and driving them simultaneously, with minimal turn-on delay difference. In general, it is best to use a gate driver with low propagation delay, and is most critical in high-frequency systems to improve efficiency.

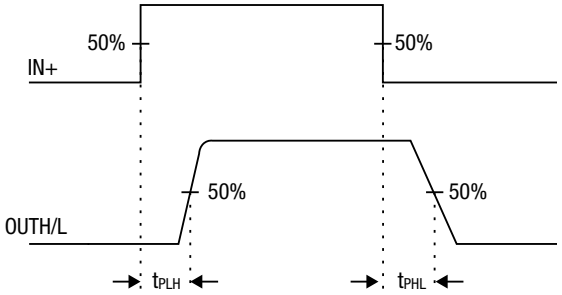


Figure 15: *Propagation delay*

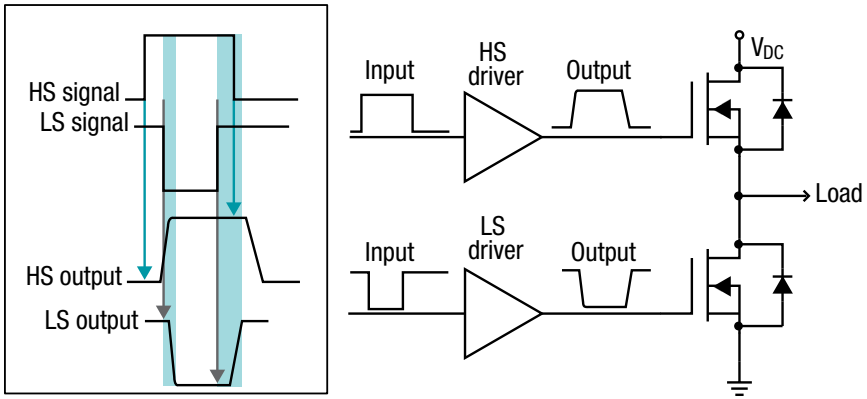


Figure 16: *Propagation delay mismatch*

Basic gate driver features

Why is it critical to have tight part-to-part propagation delay matching?

Propagation delay is a critical parameter in power systems when using multiple drivers to drive synchronous switches in power supplies and inverter applications. The delay affects how much dead time to design into the system in order to prevent two devices from turning on at the same time, or to drive multiple paralleled devices at the same time. Dual-channel gate drivers, which have an output for both the upper and lower switch, could have variations in propagation delay between the high- and low-side outputs. However, it is also common to use two single-channel drivers, as shown in **Figure 17**, so that they can be placed closer to the power devices. If the two drivers have the same propagation delay specification, then you can design the dead time to match that specification with some margin for error. The propagation delay could also be specified as a wide range due to differences between devices; for example, if the high-side driver has a longer propagation delay than the low-side driver. **Figure 18** shows an example of mismatched propagation delay and rise and fall times, which cause overlap during some of the switching cycles even with some dead time. In this case, you will need to increase the dead-time setting with a large margin to prevent shoot-through, and as a consequence reduce the converter efficiency. However, if the drivers have tight part-to-part propagation delay matching, you can decrease the dead time without having to sacrifice efficiency or worry about safety.

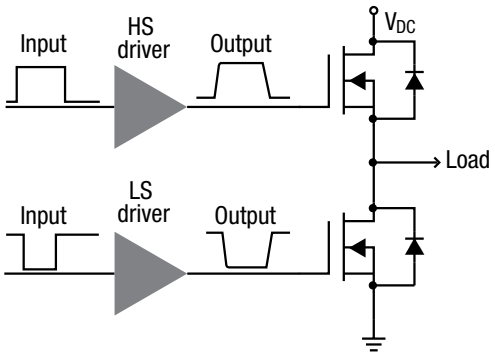


Figure 17: *Hard-switched half-bridge configuration*

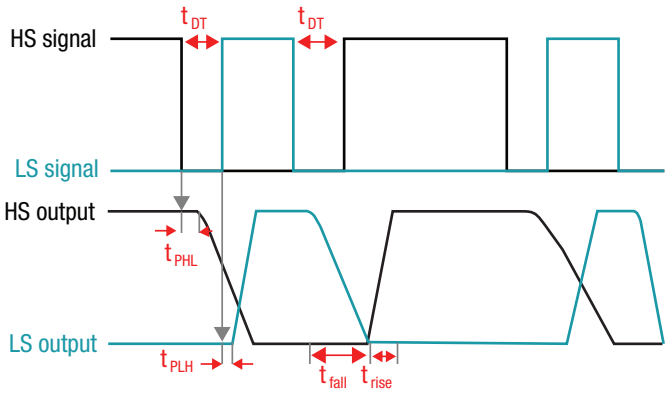


Figure 18: *Propagation delay effects on dead time*

Basic gate driver features

Why is high UVLO important for safe IGBT and SiC MOSFET power switch operation?

UVLO monitors the supply pins of a gate driver to make sure that the voltage remains above a certain threshold to ensure proper operation. On the secondary side, the UVLO rating sets the minimum allowable drive voltage to turn on the power switch. The gate voltage has effects on both conduction losses and switching losses. The switching losses will increase when V_{GS} is smaller because the available gate current is reduced, making switching slower:

$$I_G = \Delta V_{GS}/R_G$$

The conduction losses are critical to system performance and are highly dependent on V_{GS}. As shown in **Figure 19**, the output characteristics of an IGBT and SiC MOSFET vary when the gate voltage decreases. For a SiC MOSFET, the change is even more apparent. For example, if the UVLO for an IGBT is 10 V, then the device will still operate with similar conduction losses to a certain current level. However, for a MOSFET, the conduction losses will be much higher compared to a higher drive voltage. The result of high conduction losses is reduced efficiency and heating, and thus reduced lifetime. A secondary concern is the gate-drive architecture. SiC MOSFETs and IGBTs often use negative voltage rails for better turn-off performance and reliability. If UVLO is referenced to VEE, then the minimum drive voltage may be even less than the specification. It is normally best to use a higher UVLO voltage to ensure low conduction losses and better reliability over time. [UVLO tech note]

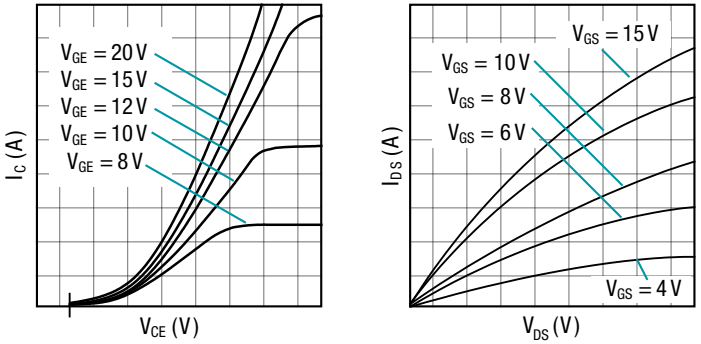


Figure 19: *IGBT and SiC MOSFET I-V curves*

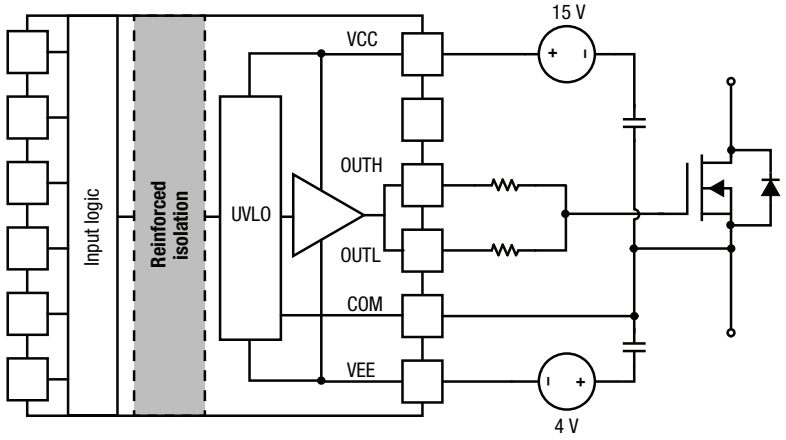


Figure 20: *UVLO referenced to COM*

Basic gate driver features

What is an input deglitch filter, and why are they important in high-power applications?

High-power applications are prone to noise from the large voltage and current transients in power switches. This noise could couple to the control signal lines tied to the gate driver. As a result, voltage spikes could occur at the gate driver inputs that are not intentional, causing the driver to turn on the power-switching device when it is not supposed to be on. The pulse may be so small that it is insufficient to fully turn on the power device, due to the input capacitance and gate resistance, and thus causes a high amount of conduction loss. If two devices are switching complementary in a half-bridge, shoot-through is a concern if they are accidentally on at the same time. Shoot-through allows high current to flow through the devices and can destroy one or both of them.

An input deglitch filter rejects noise from the environment so that the driver output does not see the glitch. Glitch rejection is typically around 20-30 ns, corresponding to a 50-MHz switching frequency, which is not near the common switching frequency for IGBT or SiC MOSFET applications. As shown in **Figures 21** and **22**, the glitch filter can reject both positive and negative pulses to prevent the device from turning on or off unintentionally. Having a deglitch filter integrated into the gate driver improves driver performance in noisy environments and protects the device from possible failure.

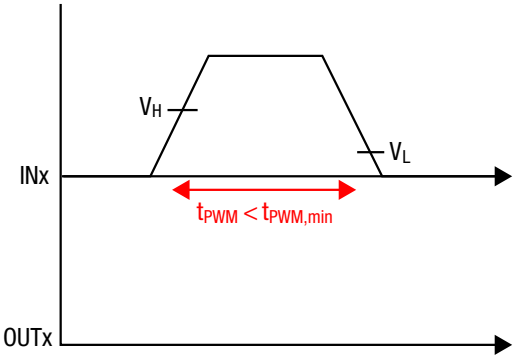


Figure 21: *Deglitch filter at turn-on*

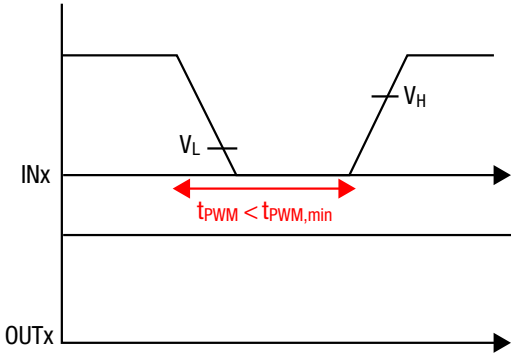


Figure 22: *Deglitch filter at turn-off*

Basic gate driver features

What is interlock protection, and how is it implemented in a driver?

IGBTs or SiC MOSFETs are critical to the operation of the system in which they operate, so it is important that they are protected. The devices are not only crucial for efficient operation; they are also one of the most costly components in a system. When devices are arranged in a half bridge, as shown in **Figure 23**, they cannot both switch on at the same time. Thus, dead time is used before the switches change states and both devices turn off. If the devices turn on at the same time, shoot-through will occur and cause a large current spike and potential failure. Shoot-through can occur in the event of an incorrect dead-time calculation that is too short, varying propagation times between drivers or noise at the input.

Interlock is a feature integrated in gate drivers to prevent shoot-through. Logic circuitry combines the positive and negative inputs of a gate driver such that they can never be on at the same time. Think of it as an integrated dead-time feature that takes delays inherent to the driver into account. Even if there is an error in the user-programmed dead time, the driver interlock will not allow both outputs to turn on. Interlock can be implemented for single-output or dual-channel drivers, as shown in **Figures 24** and **25**. In a dual-channel driver, the input channels are tied together internally; in single-output drivers, the inputs are tied together externally.

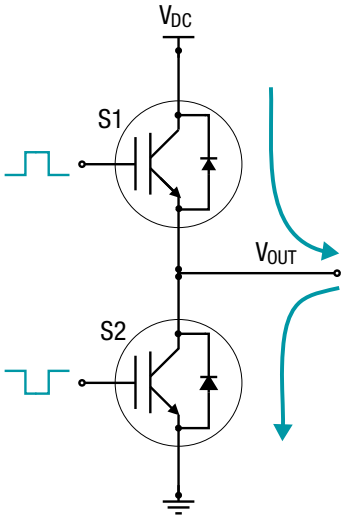


Figure 23: *Hard-switched half bridge*

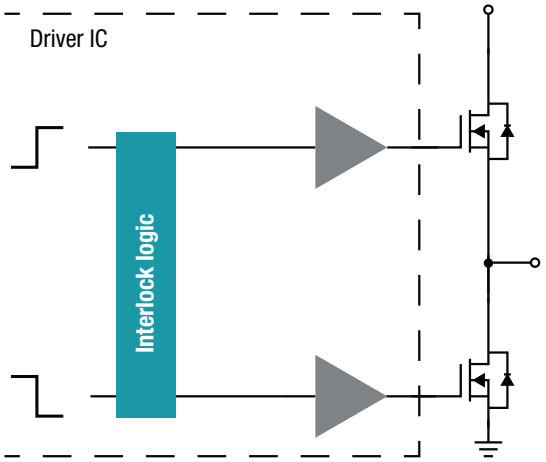


Figure 24: *Dual-channel driver with interlock*

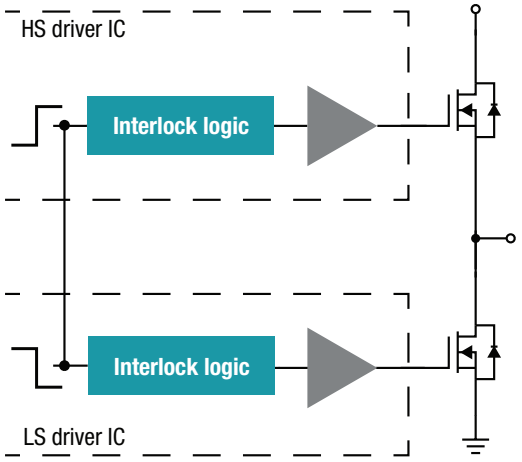


Figure 25: *Two single-channel drivers with interlock*

Basic gate driver features

Why is temperature sensed in a power converter?

Discrete power switches and power modules are designed to operate within a certain temperature range – typically -50°C to 150°C – due to packaging material limitations. However, power losses caused by switching and conduction losses will cause the die to heat up, resulting in its damage over time or complete destruction. The environment where the device operates may include extreme heat, which can also contribute to excessive die temperatures. Typically, power system designers will first de-rate the power if the temperature reaches a certain limit, and then completely shut down the converter if the temperature exceeds a maximum threshold. In order to do this, temperature sensors monitor the device temperature.

Temperature measurement accuracy is a key factor because it is not desirable to de-rate the power if it is not necessary. If the accuracy is bad, the device may still experience too much heat and degrade over time. Highly accurate measurements also provide room for margin when reducing cost in a heat-sink design.

Temperature is typically monitored using a thermistor or thermal diode. Negative temperature coefficient (NTC) thermistors often monitor temperatures in IGBT power modules, and are integrated to be physically close to the devices in order to provide the most accurate readings (**Figure 26**).

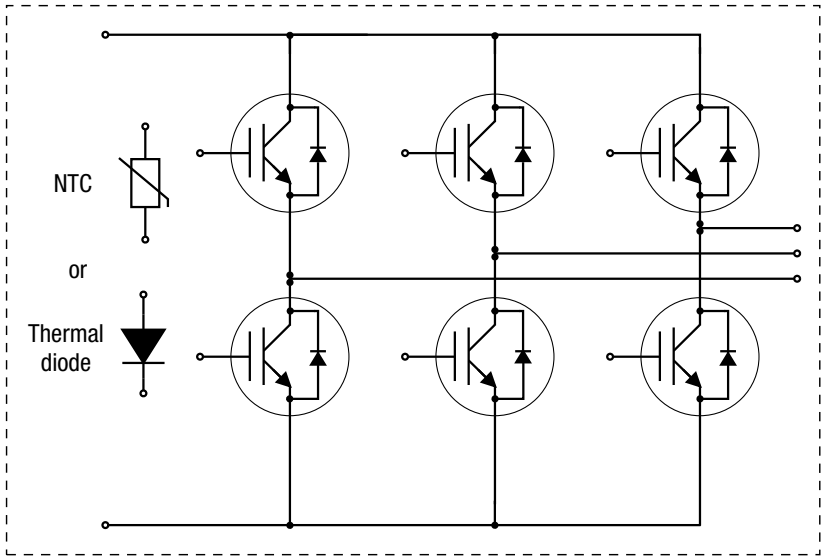


Figure 26: *Power module with integrated temperature sensors*

Basic gate driver features

What is CMTI, and how is it measured?

Common Mode Transient Immunity (CMTI) is a key specification for isolated gate drivers. CMTI is the maximum tolerable rate of the rise or fall of the common-mode voltage, V_{CM}, applied between two isolated circuits, as shown in **Figure 27**,in units of kilovolts per microsecond (kV/us) or volts per nanosecond (V/ns). To vary the slew rate for testing, either the voltage is increased or the time interval can be decreased. This isolation rating is different from other static isolation or surge ratings because it is applied at a much faster rate of change. High power switches are able to change voltage and current within hundreds of nanoseconds – or in the case of SiC MOSFETs, within 100 ns. This generates very large voltage transients, commonly >100 V/ns. The gate driver experiences these voltage swings at every switching instant, particularly when the driver is referenced to the switch node, as shown in **Figure 28**.Thus, the driver needs to be able to withstand CMTI above the rated level to prevent noise on the low-voltage circuitry side, and to prevent failure of the isolation barrier.

More on CMTI for isolated gate drivers

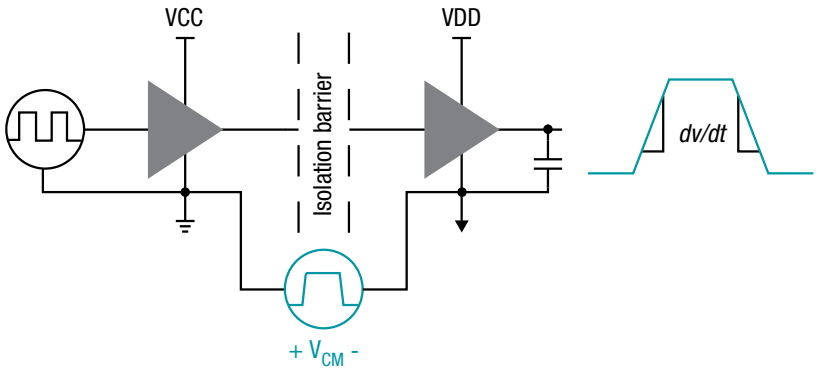


Figure 27: *CMTI test*

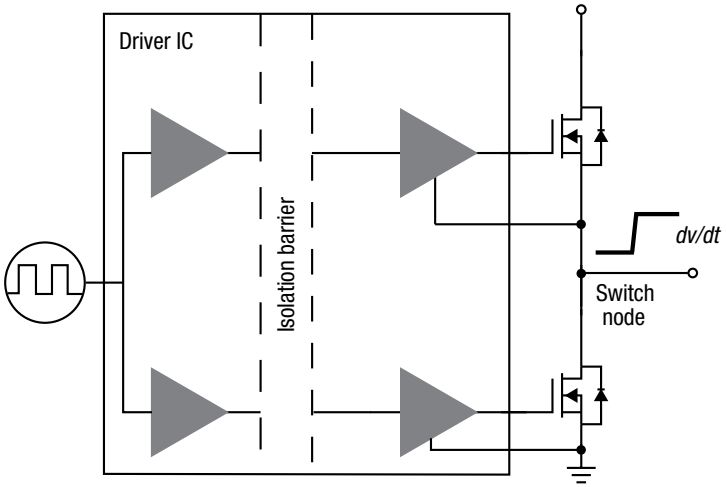


Figure 28: *Isolated dual-channel driver*

Basic gate driver features

Why is isolated sensing important, and how accurate does it need to be?

Power converters and inverters use sensors for voltage, current and temperature to provide feedback control, optimize system performance or prevent failure. For example, a three-phase motor drive uses current feedback to adjust the speed and torque of the motor. If the current measurement is not accurate, the motor will have torque ripple and will not operate properly.

As shown in **Figure 29**, it is possible to measure various signals in a system, including phase current, voltage and temperature. For both functional and safety reasons, these signals are isolated to divide the low-voltage control side from the high-voltage sensing side. The phase current is measured across a shunt on the phase line using a shunt resistor in low current systems, where the reference node is at the switch node of the inverter. If this signal is not isolated, the control side will see the high-voltage swinging of V_{DC} and the low-voltage circuitry will be damaged. Additionally, the control box may be accessible by humans, and thus high-voltage isolation is necessary to prevent electric shock.

Measurement accuracy depends on the system requirements. Typically, current and voltage must be the most accurate – within ±1% – because they are fed back to the controller to directly improve the system output. Generally, temperature is not required to be as accurate; within ±3% to 5% is sufficient to prevent failure due to overtemperature, or de-rate power to cool the system.

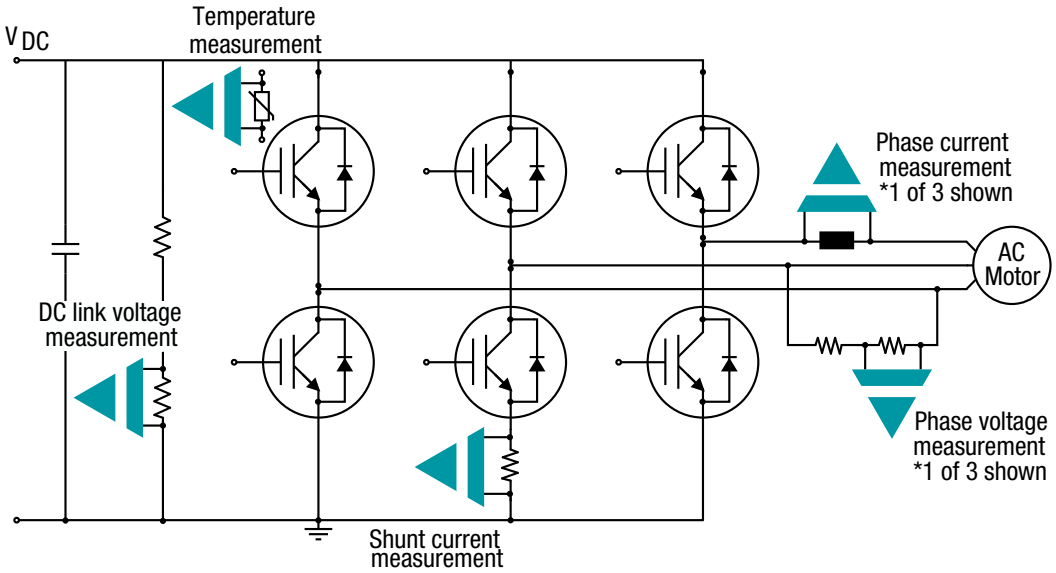


Figure 29: *Isolated sensing in a three-phase motor-drive system*

IGBT and SiC protection basics

- What is dv/dt-induced turn-on?
- What is a Miller clamp?
- What are the differences between internal and external Miller clamps?
- What is short-circuit current?
- What are the ways to detect a short circuit?
- Why is fast short-circuit fault feedback critical?
- What is desaturation in an IGBT, and how do you detect it?
- What is blanking time in the context of desaturation detection of an IGBT?
- How is a desaturation circuit designed for an IGBT?
- Why does it make more sense to detect desaturation for IGBTs than it does for SiC?
- What is overcurrent detection, and why is it more suitable for a SiC MOSFET?

Active Miller clamps

What is dv/dt-induced turn-on?

IGBTs and SiC MOSFETs are often used in high-power inverter, converter and motor-drive applications. As a result of the high power levels and these fast-switching devices, large dv/dt and di/dt will occur at each switching instance. In an ideal world, these fast transients would be beneficial to the system and would not cause any negative impact. In reality, the circuit and switching devices contain parasitic capacitances and inductances that interact with these transients, and the result could be destructive to the system.

Specifically, dv/dt can cause shoot-through by falsely turning on the lower device, S2, in a half bridge when the upper device, S1, is on as shown in **Figure 30**. The rapid increase in V_{ds} or dv/dt results in current through the parasitic capacitance C_{gd} or C_{ge}, known as the Miller capacitance, located inside the MOSFET, taking the path shown in **Figure 31**. This is given by the relationship:

$$i = C_{gd} = \frac{V_{ds}}{\Delta t}$$

The Miller current induces a voltage at the gate, dependent on the gate resistance and ratio of C_{gd} to C_{gs}. If the voltage drop is larger than the threshold voltage, V_{th}, as shown in **Figure 32**, then the device could turn on and cause shoot-through, resulting in excessive current and power dissipation.

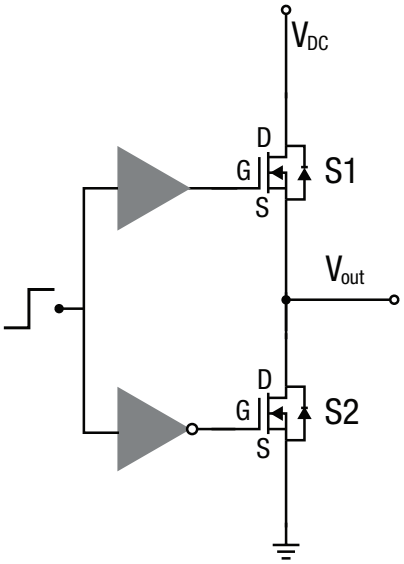


Figure 30: *MOSFET half bridge*

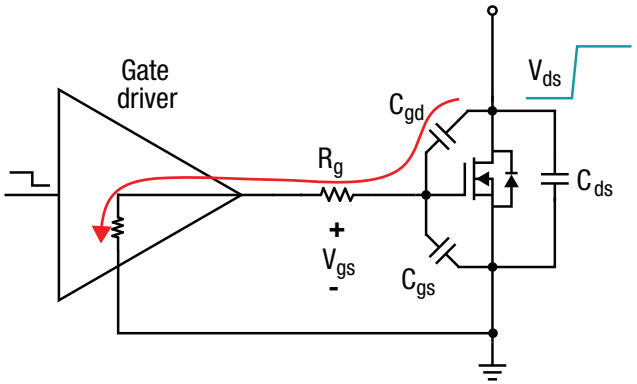


Figure 31: *Miller current path of S2*

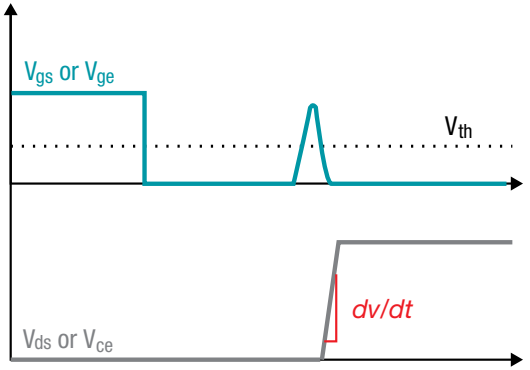


Figure 32: *Affect of Miller current on the gate voltage of S2*

Active Miller clamps

What is a Miller clamp?

The voltage transient of a power switch, dv/dt, interacts with the parasitic Miller capacitor, C_{gd}, resulting in current flowing through the gate and potentially causing false turn-on. The Miller capacitor is a fixed parameter based on the power device's physical characteristics and cannot be altered. The next solution is to reduce the dv/dt. Commonly, the gate resistor, R_g, is tuned to adjust the drive strength to reduce the switching speed to an acceptable level. However, increasing R_g also increases switching losses by slowing down the switch. Miller clamps can redirect the current without affecting the switching efficiency.

Named after the Miller capacitor, a Miller clamp is a low-impedance switch that redirects the current induced by dv/dt. The Miller clamp keeps the device in the off state, either by connecting the MOSFET's gate to ground or to a negative voltage rail. Some of the main considerations for implementing a Miller clamp are the location and the pull-down current capability. The location determines the impedance, and thus the effectiveness of the clamp; the higher the impedance, the less effective it is. The pull-down capability determines if the clamp is capable of redirecting enough of the current generated by C_{gd} to prevent a false turn-on. If the pull-down current is too small, then the clamp is not effective.

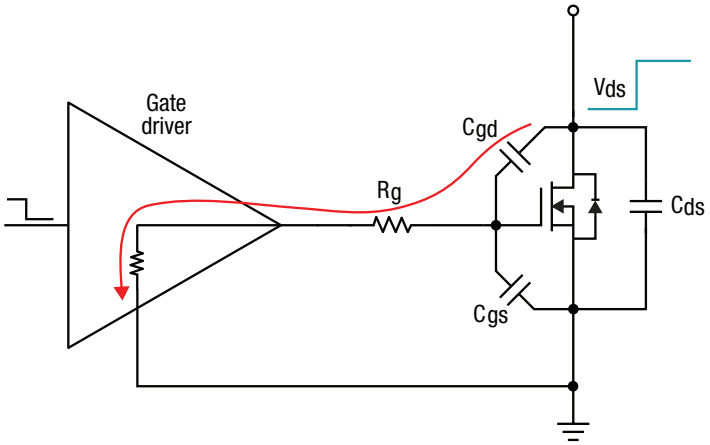


Figure 33: *Gate driver without Miller clamp*

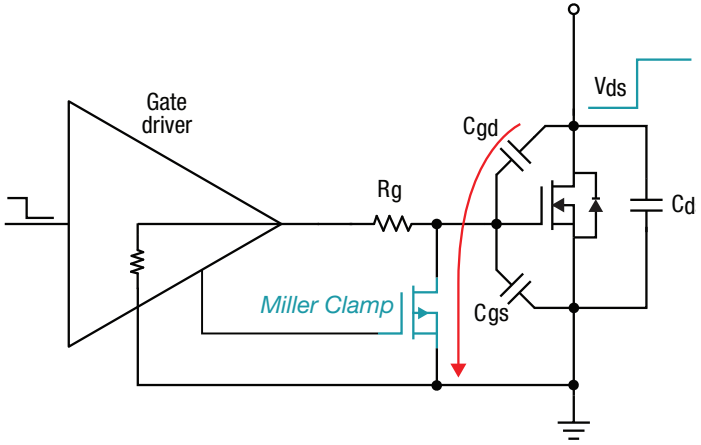


Figure 34: *Gate driver with Miller clamp*

Active Miller clamps

What are the differences between internal and external Miller clamps?

The location of a Miller clamp will greatly influence its effectiveness. The purpose of the clamp is to provide a low-impedance path for the Miller current to travel to ground. If the clamp is located far away from the switching device and the layout is not optimized, there may be more impedance in the path of the clamp than through the gate driver. It is important to evaluate whether an internal or external Miller clamp is necessary based on the system.

An internal Miller clamp is located inside the driver IC. Using an internal clamp reduces the components required to make the circuit, but it may be located far away from the power switch. It is possible that parasitic resistance and inductance, R_p and L_p, is in the path of the Miller current, as shown in **Figure 35**. If the current is large enough, the Miller clamp will not make much of a difference in driver performance.

An external Miller clamp is controlled by the driver but is located externally, as shown in **Figure 36**. In this way, the clamp may be placed very close to the power switch in order to reduce any impedance in the current path. This implementation is best for devices with high dv/dt.

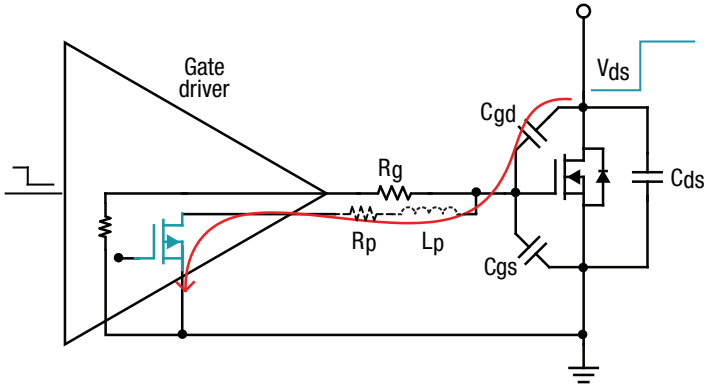


Figure 35: *Gate driver with internal Miller clamp*

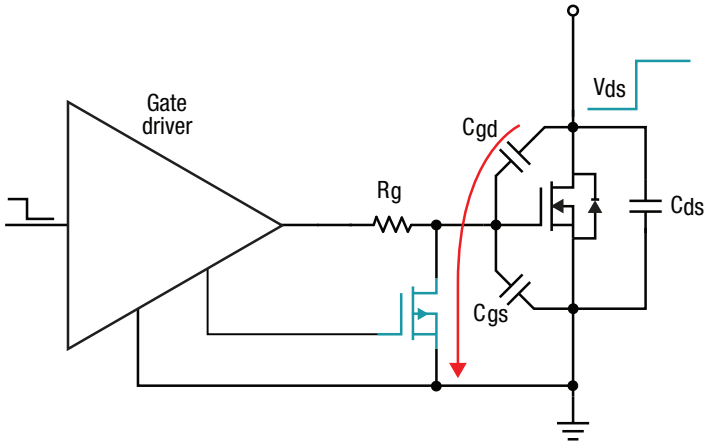


Figure 36: *Gate driver with external Miller clamp*

Short-circuit protection

What is short-circuit current?

A short circuit occurs when an electrical connection is made between conductors of differing potential, creating a path of little to no impedance. In this state, current is no longer limited and may reach a damaging level. Short circuits can occur due to a variety of reasons, including bad wiring, overload conditions or control malfunctions.

Short circuits are one of the most prevalent failures in power-electronics systems like inverters, converters and motor drives. Short circuits can lead to the catastrophic failure of power-switching devices. Switches such as IGBTs or SiC MOSFETs have a limited capability to withstand current based on their thermal capacity. Excessive short-circuit currents – much higher than the rated level – will cause a large amount of heat dissipation in the die. In **Figure 37**, V_{DC} is shorted to V_{OUT} through S1. When S2 turns on, the short-circuit current increases rapidly through the switch, as shown in **Figure 38**, leading to overheating and destruction. Thus, it is necessary to use protection circuits to detect when a short circuit occurs and subsequently shut down the power devices before a failure. The protection circuit is designed based on the allowable current level and the period of time the device can withstand an overcurrent event.

IGBT/SiC MOSFET short-circuit protection

IGBT/SiC MOSFET protection

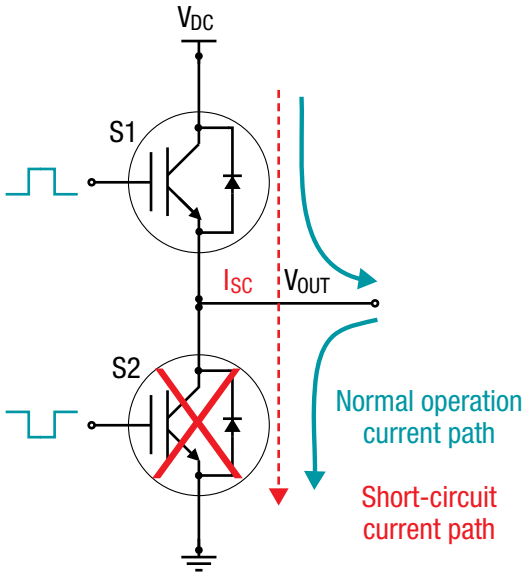


Figure 37: *Hard-switched half bridge with nonoverlapping inputs*

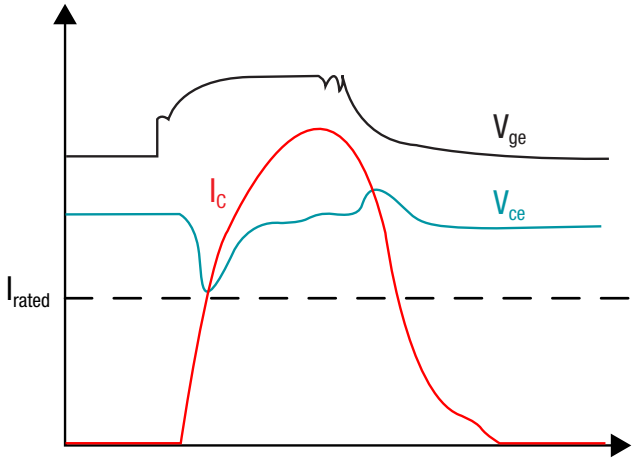


Figure 38: *Waveforms of S2 during a short-circuit event*

Short-circuit protection

What are the ways to detect a short circuit?

There are a variety of ways to detect a short circuit. The choice of method depends on the type of power device, the system voltage and current ratings, the accuracy requirements, and the cost constraints. Short-circuit sensing is all about measuring the current through the IGBT or SiC MOSFET, either directly or indirectly. See **Table 4**.

Method	Benefits	Drawbacks
V_{DS}/V_{CE} sensing (DESAT)	Simple	IGBT-specific Delay due to blanking time
Shunt resistor	Accurate	Higher power loss
Current scaling	Accurate	Limited modules with integrated current scaling available
Inductive or di/dt sensing	Fast response	Must have sensitive sensing circuitry
Gate charge	No high-voltage components required because sensing is at the gate voltage; fast response	SiC and IGBTs differ, and gate voltage can vary from device to device
Current transformer or Rogowski coil	Isolated from the circuit	Requires sensitive and high-bandwidth equipment; costly

Table 4: *Benefits and drawbacks of short-circuit detection methods*

Short-circuit protection

Why is fast short-circuit feedback critical?

Fast-short circuit feedback is critical in order to keep a device within its safe operating area. When a short circuit occurs, the current increases rapidly past the device's rated value, resulting in heating due to power dissipation. Based on the current level and the time it remains at that level, the device could be destroyed. The power dissipated in a given time period is called the short-circuit energy, as shown in **Figure 39**, and the minimum energy a device can withstand is called its critical energy, E_C.

E_C is not always clearly defined, but you can make an estimation from the plot of the junction-to-case thermal impedance, Z_{thjc}, like the one shown in **Figure 40**. This plot shows the Z_{thjc} (°C/W) versus the pulse time, t_p, and at varying duty cycles, D. The thermal impedance is critical because it defines the thermal capacity of the die. Typically, a device is required to stay below a specified junction temperature, T_j, and the critical energy is calculated as:

$$E_C = \frac{T_j}{Z_{thjc}} * t_p$$

The pulse width can help determine how fast the short-circuit feedback circuit must be in order to prevent the device from overheating. This is even more critical for SiC MOSFETs because of their fast switching, where current can increase very rapidly, and because of their small die size, giving them a lower short-circuit withstand time (SCWT) compared to an IGBT. Thus, it is critical to reduce the time to measure an overcurrent event, and choose the proper protection circuitry to do so.

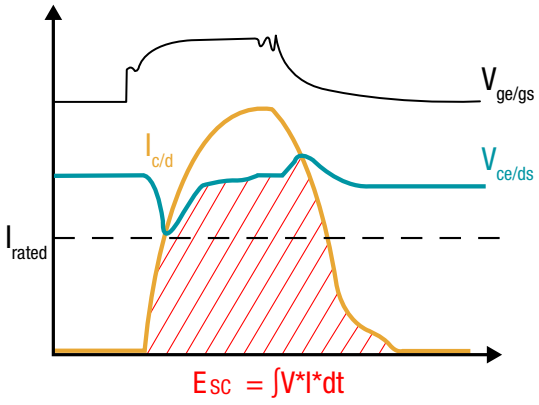


Figure 39: *Power loss during a short circuit*

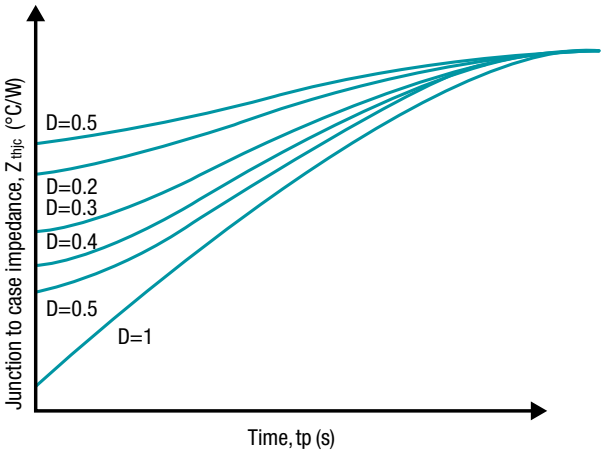


Figure 40: *MOSFET thermal impedance for a single pulse*

Short-circuit protection

What is desaturation in an IGBT, and how do you detect it?

Overcurrent in an IGBT causes desaturation. Desaturation can be caused by a variety of short-circuit events where current rapidly increases past the device's maximum rating. When the IGBT desaturates, moving from saturation to the active region, maximum power is dissipated, resulting in overheating and possibly catastrophic damage. Thus, it is crucial to operate the IGBT within the saturation region by limiting the current, I_c.

At the current knee, shown in **Figure 41**, the device begins transitioning into the active region. At this point, I_c stops increasing while V_{ce} continues to increase. Protection circuits are designed to detect this transition, either by measuring current or by monitoring the voltage level at preset thresholds, I_{DESAT} or V_{DESAT}, respectively. The most popular protection circuit is called DESAT protection, which monitors the on-state voltage, V_{ce}, to detect when the threshold is reached. In this case, V_{DESAT} is chosen to be within the current knee region, typically 7 V to 10 V. During normal operation, $V_{DESAT} > V_{ce}$.

When $V_{DESAT} < V_{ce}$, DESAT is triggered, and the circuit will safely shut down the IGBT in order to prevent damage to the device. The DESAT circuit may be integrated into the gate driver or implemented using discrete components.

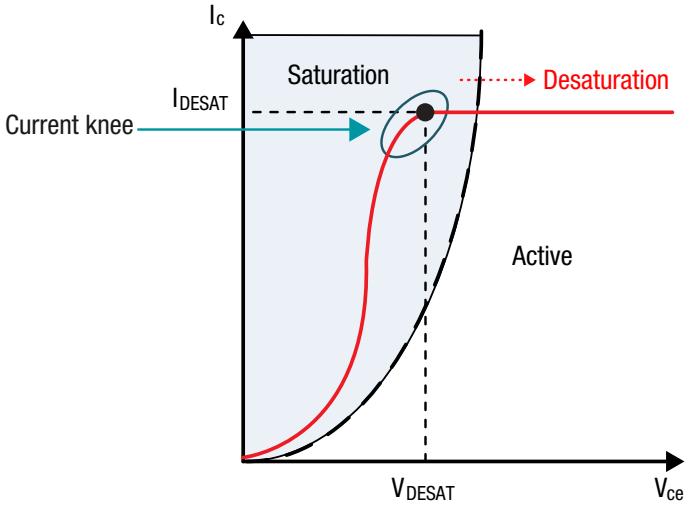


Figure 41: *I-V curve of an IGBT*

Short-circuit protection

What is blanking time in the context of desaturation detection of an IGBT?

DESAT detection must trigger fast enough to prevent catastrophic failure. However, immediate DESAT detection could result in an inaccurate fault trigger due to system nonidealities such as nonideal switching of the power device, where the voltage and current transitions can take hundreds of nanoseconds to complete. As shown in **Figure 42**, current rises first, then the voltage falls. DESAT detects the voltage, V_{ce} or V_{ds}, during the on-state, so the measurement should be delayed until the device is fully turned on and the voltage reaches its lowest value. Additionally, oscillations can occur after the fast voltage transient, causing the DESAT voltage to rise above the threshold. For these reasons, DESAT circuits are designed with an inherent delay called the blanking time, and should be at least t4-t0.

As described, the blanking time, t_{BLK}, should be long enough to prevent a false trip, yet short enough to shut down the device before it gets damaged.

The recommended blanking time is typically ~2 µs, which is less than the IGBT's SCWT. SCWT is defined by the maximum allowable power dissipation for a given time period. The DESAT circuit is designed using the components shown in **Figure 43**, which include a current source, I_{CHG}; a voltage reference, V_{DESAT}; and a capacitor, C_{BLK}. The blanking time is calculated as:

$$t_{BLK} = \frac{C_{BLK} * V_{DESAT}}{I_{CHG}}$$

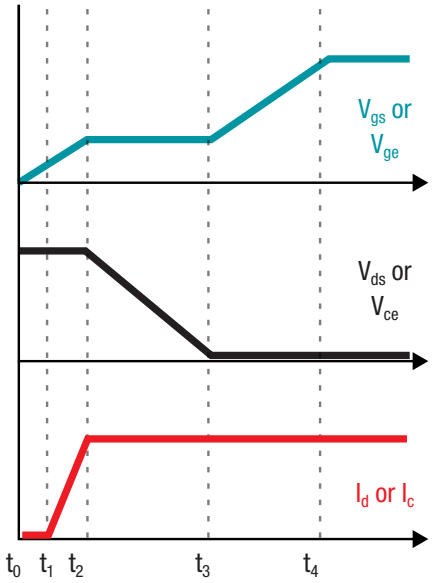


Figure 42: *Power switch turn-on waveforms*

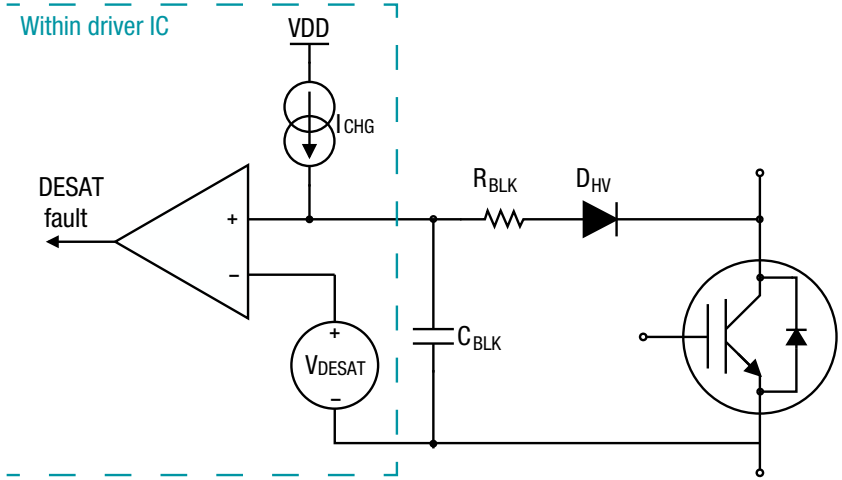


Figure 43: *Typical DESAT circuit implementation*

Short-circuit protection

How is a desaturation circuit designed for an IGBT?

DESAT protection circuits require consideration to properly set the blanking time, DESAT threshold voltage and high-voltage blocking diode. The blanking time, t_{BLK}, must be long enough to prevent a false trigger, but shorter than the device's SCWT. The setting of the blanking time depends on the IGBT's characteristics. The charge current, I_{CHG}, is typically provided in a driver IC with DESAT functionality, as well as the threshold voltage, V_{DESAT}, as shown in **Figure 44**.

The high-voltage diode, D_{HV}, is set based on the DC bus voltage. D_{HV} could be multiple diodes in series when V_{DC} is in the kilovolt range. The reverse recovery of D_{HV} should be minimal to prevent reverse current from causing a false trip. It is best to use fast-recovery diodes to prevent a false DESAT fault signal. Additionally, multiple high-voltage diodes can help adjust the actual threshold voltage, $V_{DESAT,actual}$, where the number of diodes times their forward voltage is subtracted from V_{DESAT}. V_{DESAT} is the reference voltage at which the DESAT fault triggers, which is set within a gate driver with integrated DESAT protection. The actual detection voltage is adjustable based the blanking resistor, R_{BLK}, and the forward voltage drop of the high-voltage diodes. You must use each of these components to accurately set the DESAT voltage. Thus, the actual detection voltage is:

$$V_{DESAT,\,actual} = V_{DESAT} - I_{CHG} * R_{BLK} - n * V_{DHV}$$

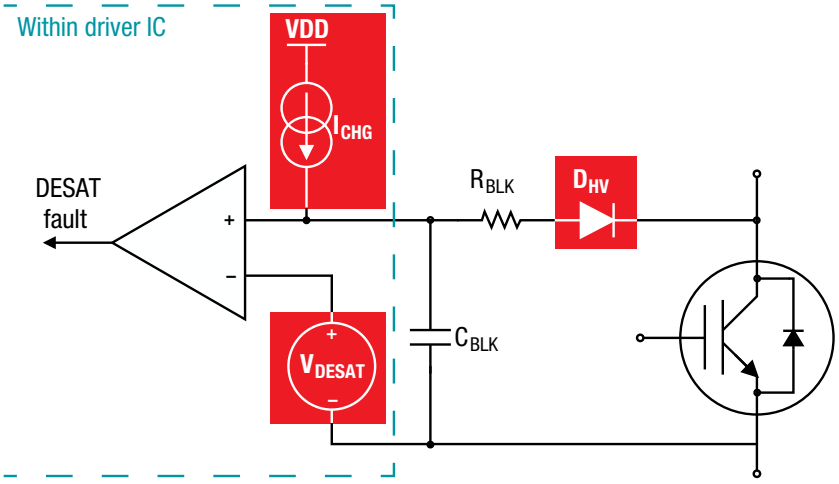


Figure 44: *Typical DESAT circuit implementation*

Short-circuit protection

Why does it make more sense to detect desaturation for IGBTs than it does for SiC?

DESAT is the most common overcurrent protection circuit and is the default choice for many applications because it is simple to implement. However, there are inherent differences between IGBTs and SiC MOSFETs that make DESAT protection better suited for IGBTs than SiC MOSFETs. **Figure 45** shows the I-V characteristics of an IGBT and SiC MOSFET. For the same rated current and voltage, the IGBT reaches the active region at a significantly lower Vce than the SiC MOSFET's corresponding Vds level as it transitions into the saturation region. Inherently, the IGBT limits the power dissipated because the current stops increasing. In the SiC MOSFET, the current continues to increase while Vds also increases, causing the device to break down at a faster rate due to high power dissipation and resulting heat. Additionally, SiC MOSFETs will reach a point of maximum power dissipation sooner than IGBTs because they switch at a much faster rate.

The desaturation voltage for an IGBT is typically 7 V-10 V, while for a SiC MOSFET, there is no clearly defined region. Choosing the DESAT voltage for an IGBT is much simpler because of this, but is nearly impossible for a SiC MOSFET. DESAT with a SiC MOSFET is possible with some adaptations but will not result in the best performance. SiC MOSFETs have a shorter SCWT than IGBTs and switch faster, so the timing is critical. Methods like shunt-resistor current monitoring or overcurrent detection are best for SiC MOSFETs.

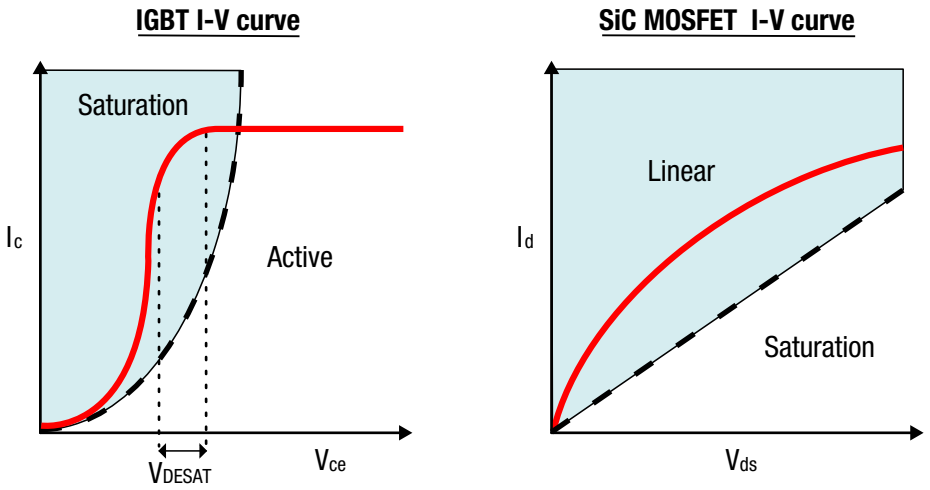


Figure 45: *I-V curves for IGBTs vs. SiC MOSFETs*

Short-circuit protection

What is overcurrent detection, and why is it more suitable for a SiC MOSFET?

DESAT as a form of short-circuit protection is common in IGBTs, but is not always a good fit for SiC MOSFETs due to its I-V characteristics. An SiC MOSFET's transition from the linear to the saturation region is not clear, so using a single voltage threshold for DESAT detection may not be very accurate. A more suitable form of detection is overcurrent detection, which measures the current through an accurate shunt resistor, R_{shunt}. R_{shunt} measurements do result in higher power losses given the high current flowing through them. As a result, they may also be less accurate, due to self-heating. The shunt resistor value is normally in the milliohms range, and the measured current is derived using Ohm's law (V = I * R). Compared to DESAT, shunt-resistor monitoring is more accurate and requires less circuitry. Less circuitry also means that the response time will be faster, which is critical for SiC MOSFETs because they have a lower SCWT than IGBTs.

To solve the issue of power loss, some power modules include integrated current scaling to reduce the current that passes through the shunt resistor (**Figure 46**). A current divider circuit built within the module reduces power dissipated in the shunt resistor and the ratio is given by the power device manufacturer. This method has less power loss than typical shunt resistor measurements and results in a more accurate current measurement.

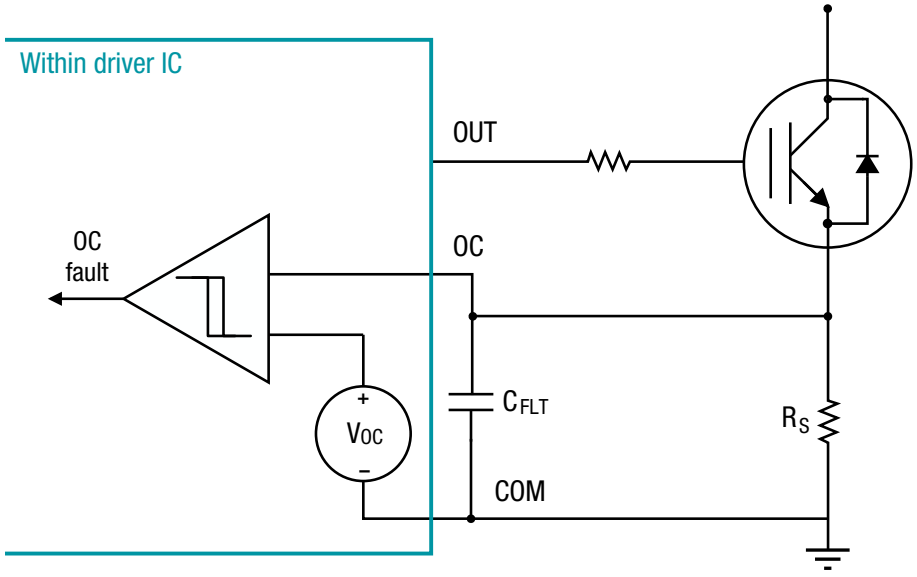


Figure 46: *Overcurrent using a FET with integrated current scaling*

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265