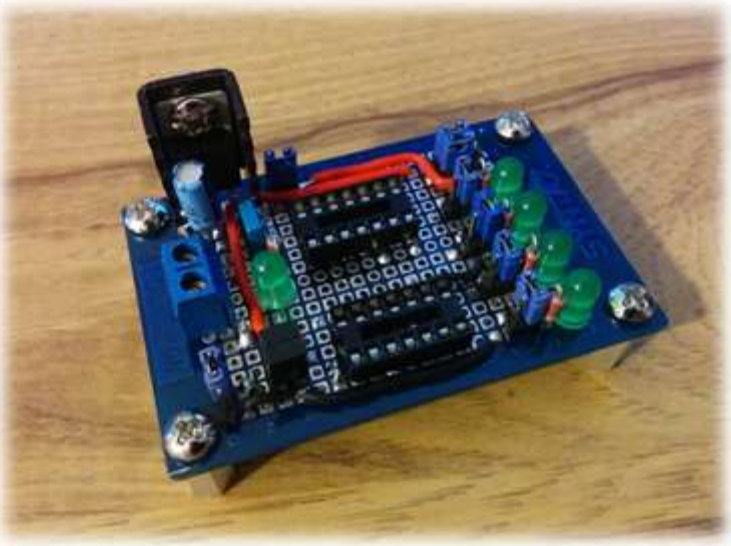
B.T.U.

Boolean Testing Unit



Testing prototype with built in DC power supply for exchangeable quad 2-input logic gates integrated circuits and truth table display

Prepared by

Daniel G Gonzalez

August 14, 2014

Table of Content

Summary

This project is meant to design and build a testing module for quad 2-input logic gates integrated circuits by eliminating construction or logic errors and factors related to the operator. The testing consists in input voltage or zero reference in proper combination through all four gates and display the expected true table from the integrated circuit; all outputs at once. If the corresponding LED doesn't turn on, or the table built is not the associated logic table to the IC, then it can be determined that the chip is not working properly. For working IC's, the outputs can be combined with a NOT logic gate integrated circuit to test different outputs.

Components

The prototype consists in an independent voltage regulator module with polarity protection, two sockets to exchange the IC's, a PIN junction to invert the polarity of the input voltage for the IC testing socket (for the NOR gate only), a PIN junction to enable and disable the sockets if required, a PIN junction per output to control a direct output from the testing IC socket or the inversed output (If the NOT IC is enabled), an ON/OFF pin connection to disable the voltage regulator, and a ON/OFF pin connection to separate the voltage regulator module from the rest of the circuit.

Voltage Regulation Module (V.R.M.)

Consists in:

a) 1 1N4006 silicon diode
b) 1 LM7805 Linear Positive 1A Voltage Regulator
c) 1 470 nF Electrolytic capacitor.
d) 1 100 nF Ceramic capacitor.
e) 1 220R carbon composite resistor
f) 1 Green LED
g) 1 clamp connection
h) 5 male pins
i) 2 2-pin female jumpers

Description and Justification

- The 1N4006 diode was used due to its high reverse voltage tolerance and because it was the accessible component at the moment of construction of the prototype.
- The LM7805 was used because it's an easy to use low power regulator. As a precaution, a heat sync was attached to it.
- The 470 nF Electrolytic capacitor was used under Dr. Hopper recommendation as an upgrade from the standard 300 nF ceramic capacitor, to improve the electric noise reduction to the input to the Voltage regulator.
- The LED is used to show an ON/OFF state of the voltage regulation module, so as to discharge the capacitors after turning the module OFF.
- The pins are used as an ON/OFF switch to the circuit and as a removable junction to the circuit; this is to add a different input voltage to the testing module or to use the voltage regulation module for another circuit.

Testing Module

Consists in:

a) Premade 20 x 15 female pin soldering board
b) 2 14 pin IC sockets
c) 4 220R carbon composite resistors
d) 4 Green LEDs
e) 21 male pins
f) 8 2-pin female jumpers
g) 4 stand offs with screws

Description and Justification

- The PIN junction P03 is used to power the sockets and the testing LEDs. The possible combinations are: enable the testing IC socket alone (Figure 1a; pins o-n), the NOT IC alone (Figure 1b; pins o-s), or both simultaneously (Figure 1c; pins o-s and e-n). On its current configuration, no other combination used will bring any change to the circuit input voltages.

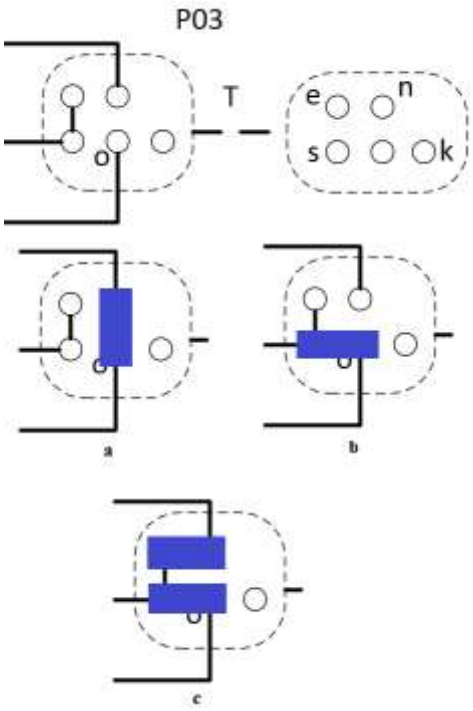


Figure 1 – PIN junction P03

- Both sockets are connected with permanent soldered connections.
- PIN junction G is used to set direct input voltage and reference into the testing socket (Figure 2a; pins x-a and pins b-y) or inverse connection (Figure 2b; pins x-b and a-y), to test a standard quad 2-input NOR gate (7402). Due to its internal configuration, only the input voltage and reference points has to be exchanged for proper connection and testing.

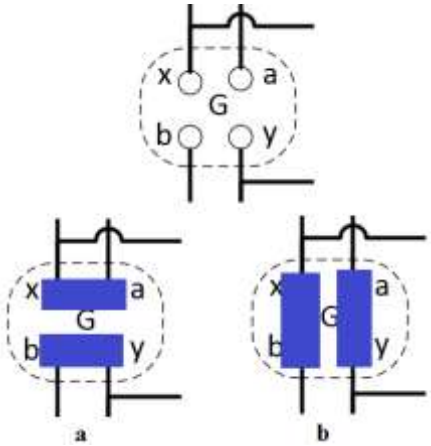


Figure 2 – PIN junction G

- When connecting an IC for testing, all the connections match the proper configuration for all the logic gates to work properly (Figure 3a). When changing the PIN junction G, the NOR gate matches the pin configuration in Figure 3b.

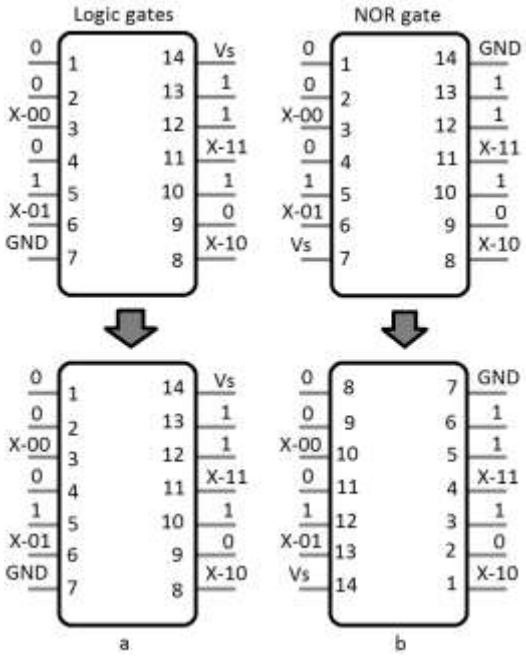


Figure 3 – Pin association within the IC testing socket

- The NOT gate is removable in case of failure. However, there design of this first prototype doesn't include testing for this unique gate.
- PIN junction P04 changes the input between the testing IC socket (Figure 4a; pin in-out) and the NOT testing socket (Figure 4b; NOT-out).

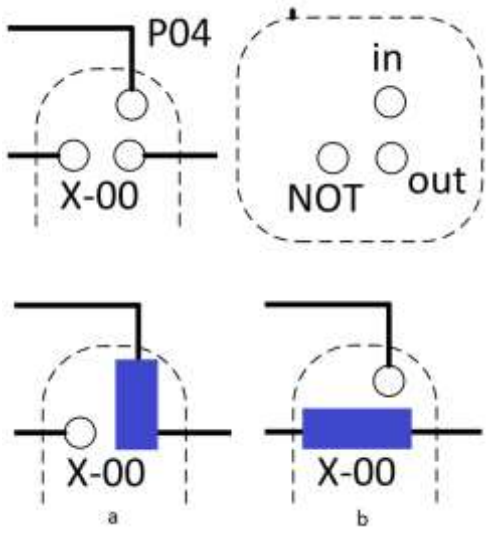


Figure 4 – PIN junction for direct or NOT output

- The four LEDs will display the logic table in the sequence 00 (D-00), 01 (D-01), 10 (D-10), 11 (D-11); from top to bottom.
- Because the board used doesn't have pre-made wiring connection, all the wiring had to be done both with #22 solid wires (color coded) and soldered jumpers. The code for the wires is:
    - Red – supply voltage / logic 1
    - Black – reference / logic 0
    - Yellow – Logic output to P04
    - Brown – Logic output to NOT input
    - Purple – NOT output to P04
    - Blue – discarded
- By recommendation of Prof. Mayer, a ceramic capacitor between the input voltage and the reference of the testing socket would reduce the electrical noise generated to the circuit in case some was generated by changing the ICs to be tested. However, because of the simplicity of this prototype, this capacitor is not required.

Conclusions

- This testing probe is a first attempt to identify logic gates through its actual output for those cases when the label is too hard to read or has completely vanished.
- If the gate is known but the output has a weird behavior, it can be a first indication that the logic gate is not working properly. This case might happen in over used ICs or a missed connection that lead to overheat.
- The current used to operate the whole circuit is relatively low, making the circuit a low power consumption tool.
- By making the voltage regulator module independent to the testing module, the VRM can be used for other circuits, so as the TM can be supplied by a different source. This can be convenient in case one of them fails.
- The output LEDs had a Light Emission "cut off" between 4.3 - 4.5 V Source Voltage.
- The pin k, from PIN junction P03, was intended to be used as a direct voltage input to the LEDs to test them. However, this connection was shorting the output of the testing sockets and had to be removed.

Limitations

- The B.T.U. doesn't include electronics able to detect shorts between connections or overheating, making it temperature vulnerable.
- It needs an external power supply to work properly.
- The pin switch for the NOR gate is necessary or the circuit will overheat and damage the circuit board and the IC.
- The NOT gate cannot be tested with this prototype.
- The board used doesn't have premade connections between components. Troubleshooting or changing a component is extremely difficult.

Upgrades

- Replace RI/O with a 330 Ω to reduce the current flowing across the I/O branch.
- Add a modification to test a NOT test, either by adding more LEDs and a modification to the output LEDs, or by another more sophisticated circuit.
- Include a protection circuit to avoid overheating or excessive current flow (in case of a short).

Electric Diagram

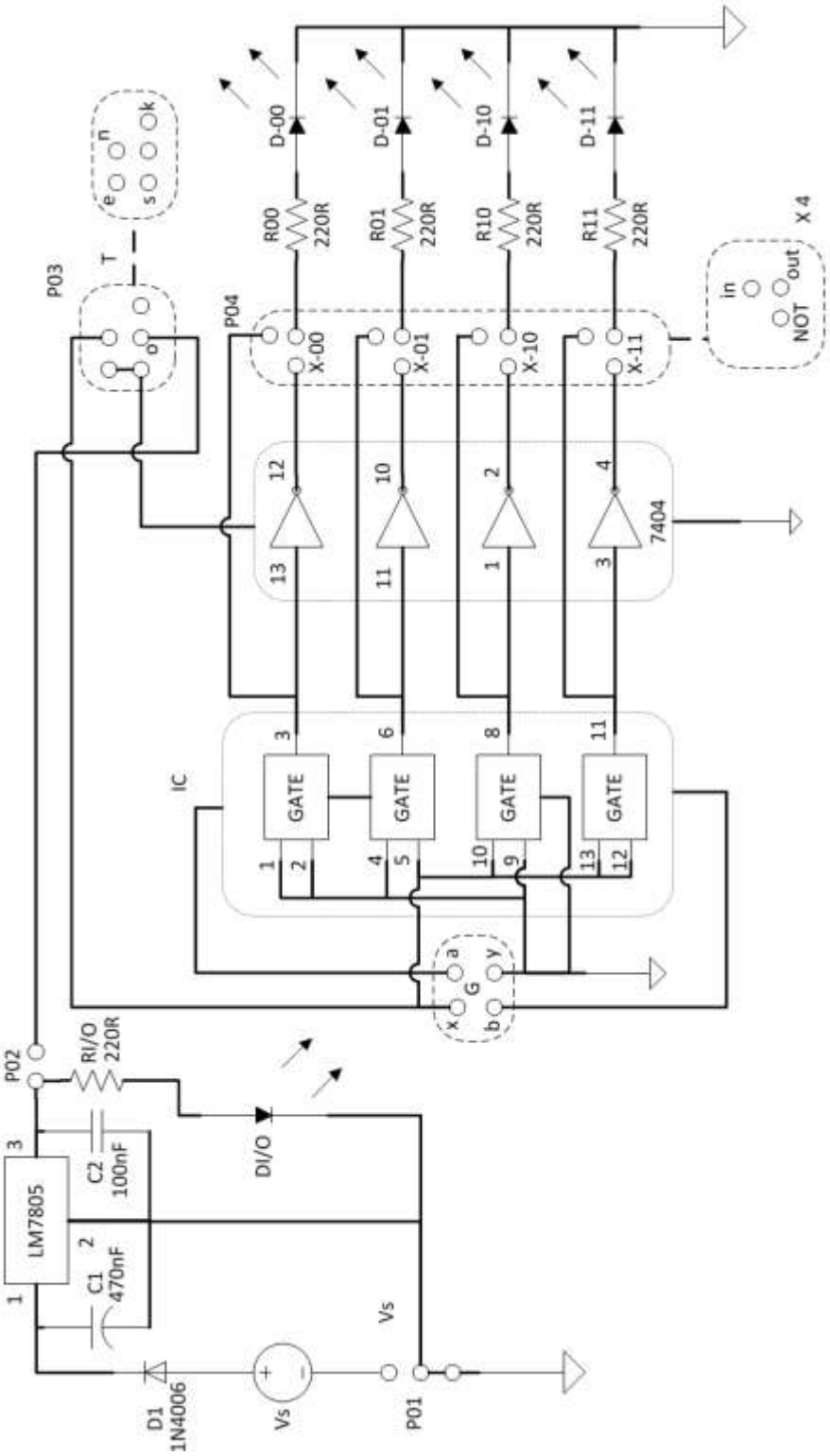


Figure 5 – Electric Diagram

Soldering Diagram

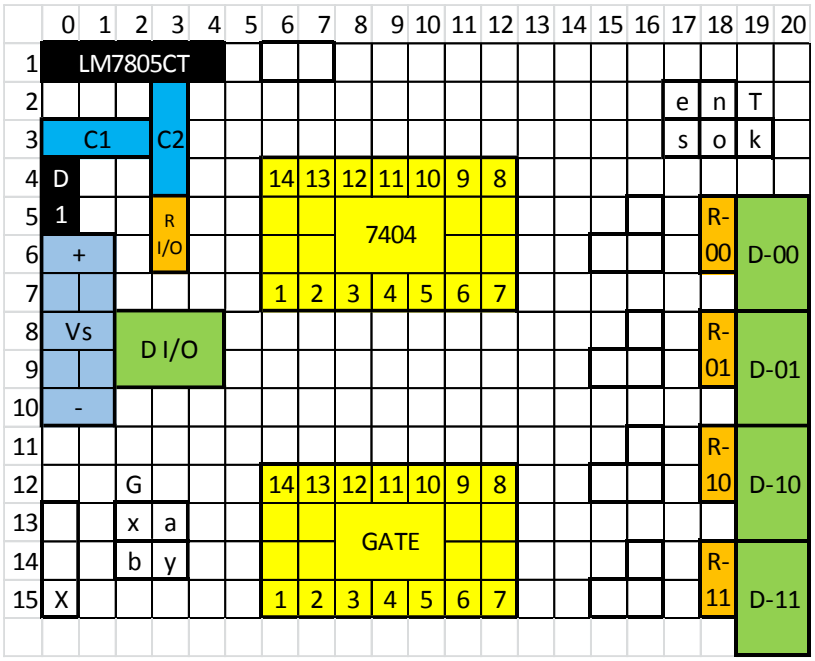


Figure 6 – Soldering board component location

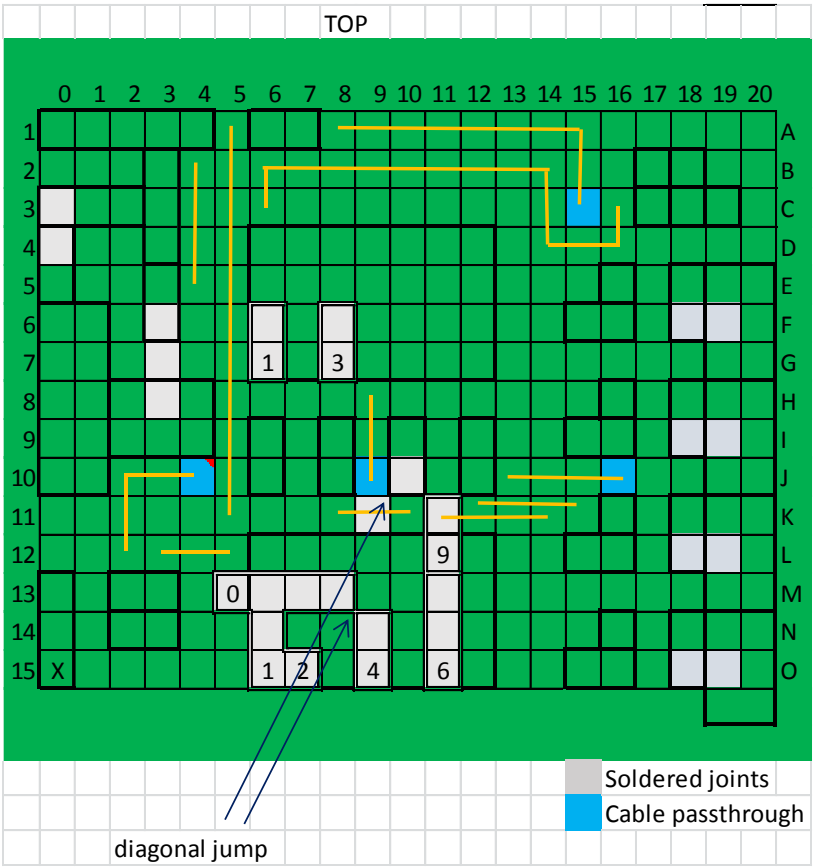


Figure 7 – Tentative top solder connections layout

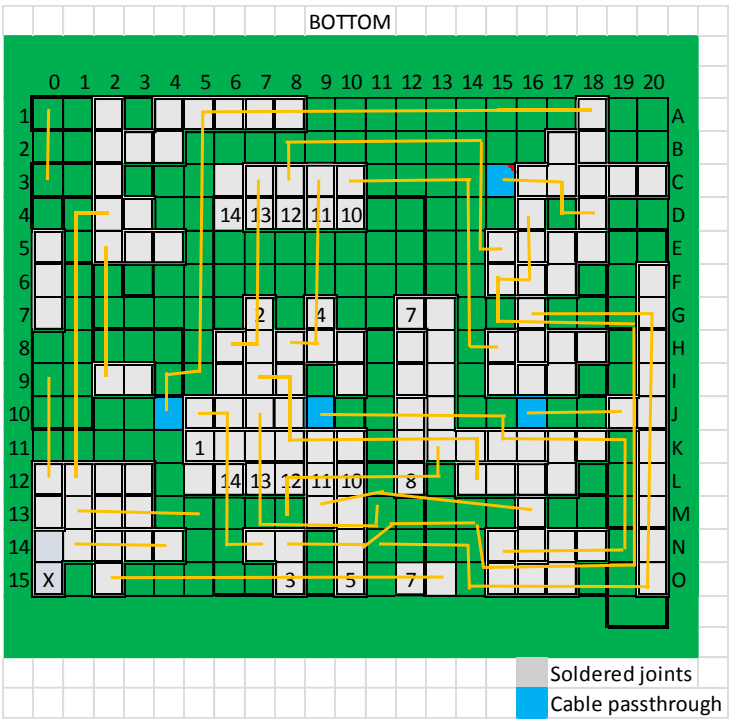


Figure 8 – Tentative bottom solder connections layout

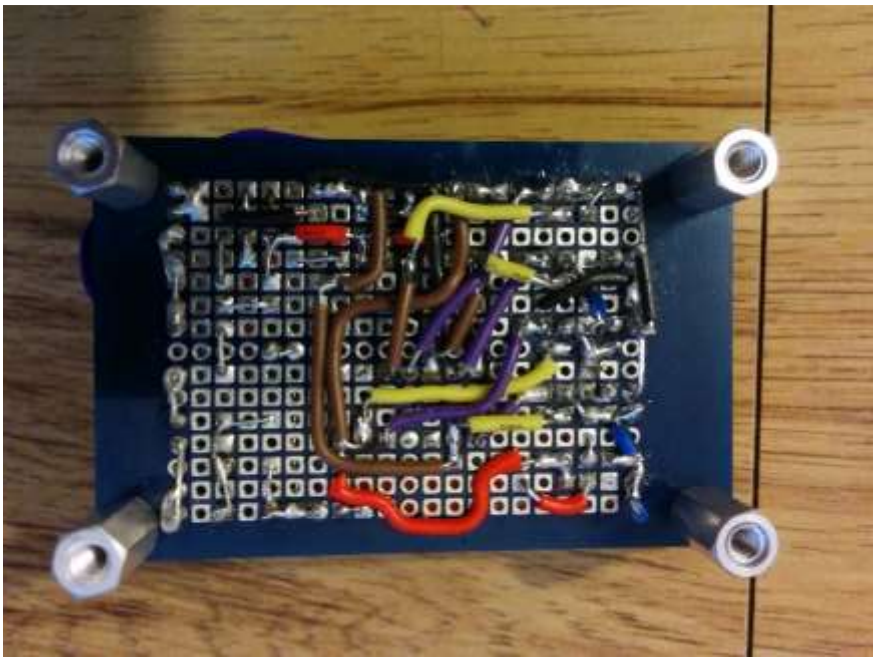


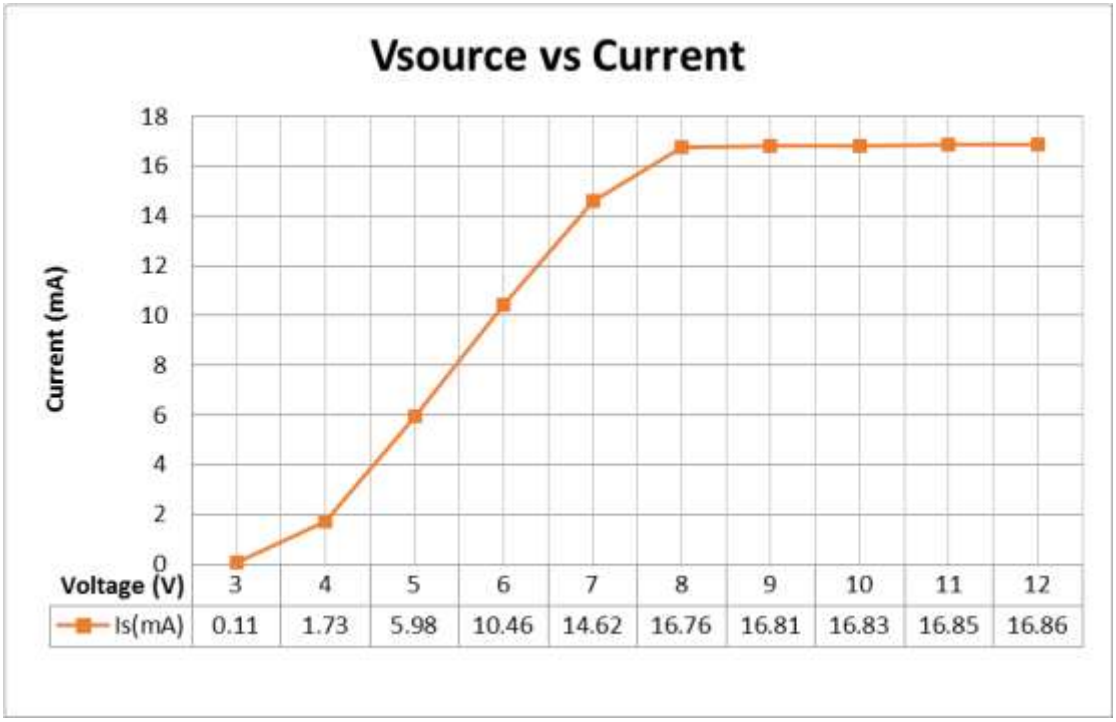
Figure 9 – Actual solder layout

Measurements

The following measurements were done using a Gw Instek GPS-3303 Laboratory DC Power Supply and a BK Precision 2831C Digital Multimeter at a room temperature around 20ºC with artificial cold illumination.

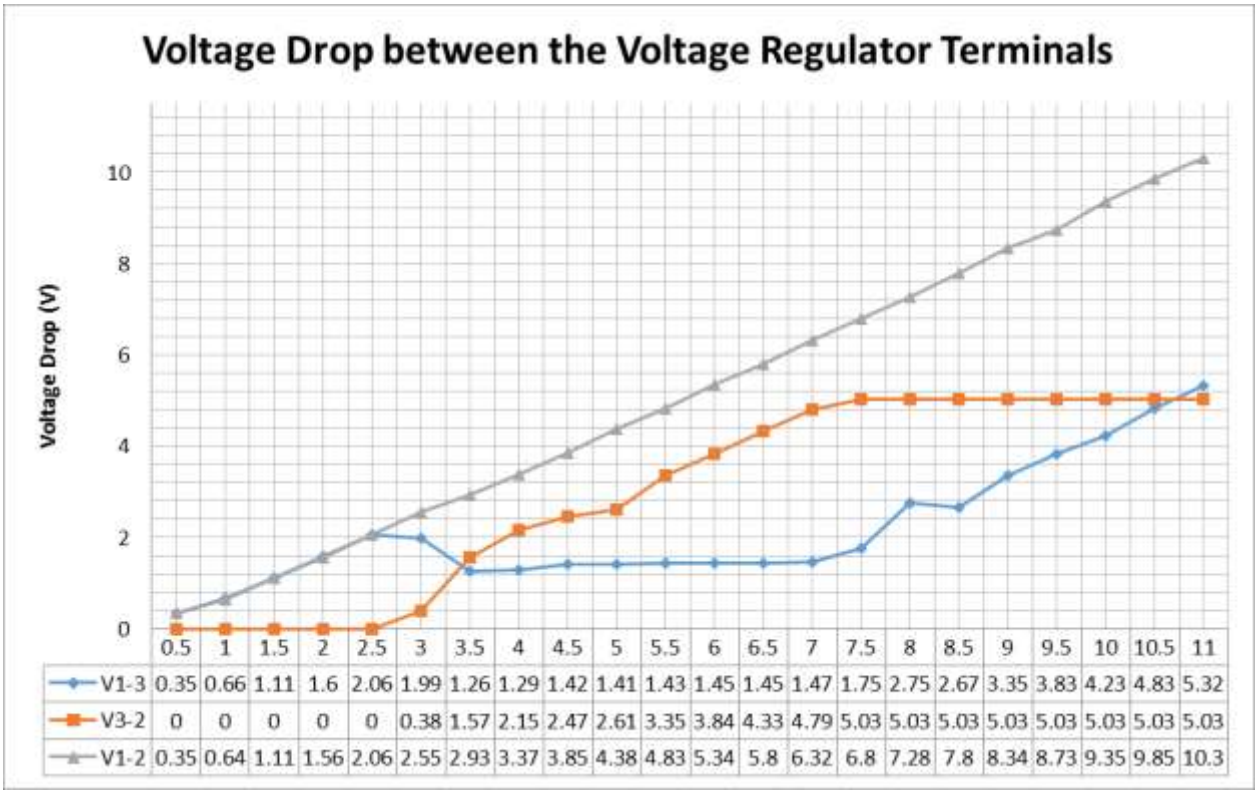
Data collected has the purpose of determining a first behavior of the components within the desired input voltage range for this circuit; that is with a 9V battery. No destructive testing was done to this prototype; maximum limits cannot be specified with the data collected.

Voltage Regulator Module



Voltage (V)	3	4	5	6	7	8	9	10	11	12
Is(mA)	0.11	1.73	5.98	10.46	14.62	16.76	16.81	16.83	16.85	16.86

Graph 1 – Voltage Regulator Voltage, no load connected. Measured through P01



	0.5	1	1.5	2	2.5	3	3.5	4	4.5	5	5.5	6	6.5	7	7.5	8	8.5	9	9.5	10	10.5	11
V1-3	0.35	0.66	1.11	1.6	2.06	1.99	1.26	1.29	1.42	1.41	1.43	1.45	1.45	1.47	1.75	2.75	2.67	3.35	3.83	4.23	4.83	5.32
V3-2	0	0	0	0	0	0.38	1.57	2.15	2.47	2.61	3.35	3.84	4.33	4.79	5.03	5.03	5.03	5.03	5.03	5.03	5.03	5.03
V1-2	0.35	0.64	1.11	1.56	2.06	2.55	2.93	3.37	3.85	4.38	4.83	5.34	5.8	6.32	6.8	7.28	7.8	8.34	8.73	9.35	9.85	10.3

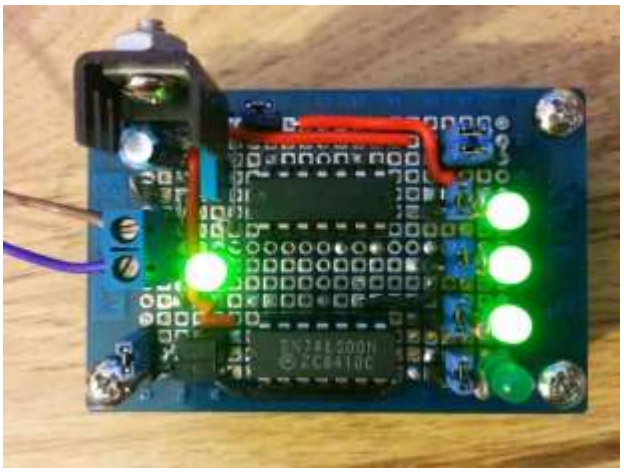
Graph 2 – Voltage drop between the Voltage Regulator Terminals.

An odd behavior can be observed for V1-3. It follows the same voltage drop as V1-2 until 2.5V is reached. Then, probably the component gets enough power to start working. By comparing V1-3 and V3-2, it might be possible that this two voltages, on nominal operation, add together to match the voltage source, keeping V3-2 almost constant (The output voltage used to power the whole circuit). V1-2 shows the source voltage minus the diode voltage drop.

Testing Module Measurements

These currents were measured across PIN junction P02.

7400 – Quad 2-input NAND gate

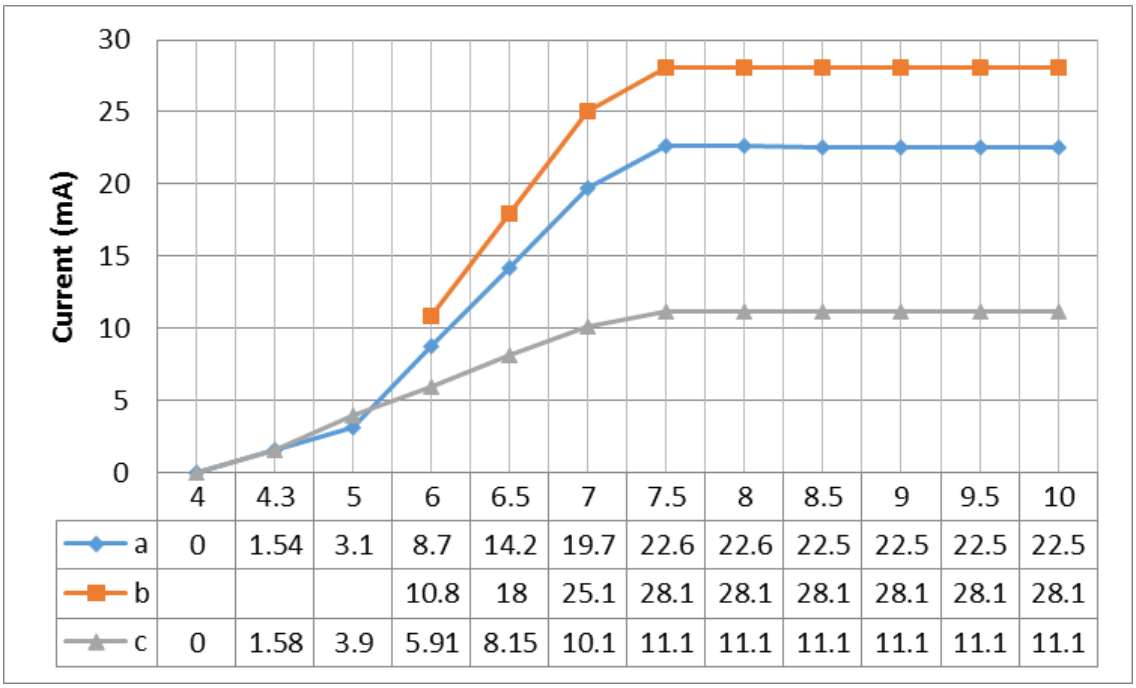


A	B	Y= (AB)'
0	0	1
0	1	1
1	0	1
1	1	0

a) Current (mA). NOT IC powered, no Inversion. 3 LED's on.

b) Current (mA). NOT IC powered, 1 inversion connected. 4 LEDs on.

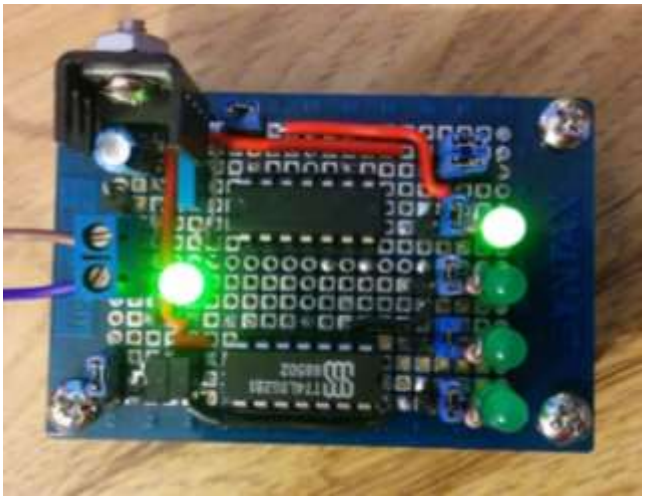
c) Current (mA). NOT IC powered, all inversions connected. 1 LED on.



	4	4.3	5	6	6.5	7	7.5	8	8.5	9	9.5	10
a	0	1.54	3.1	8.7	14.2	19.7	22.6	22.6	22.5	22.5	22.5	22.5
b				10.8	18	25.1	28.1	28.1	28.1	28.1	28.1	28.1
c	0	1.58	3.9	5.91	8.15	10.1	11.1	11.1	11.1	11.1	11.1	11.1

Graph 3 – 7400 NAND gate current tendencies vs. Source Voltage Vs

7402 – Quad 2-input NOR gate

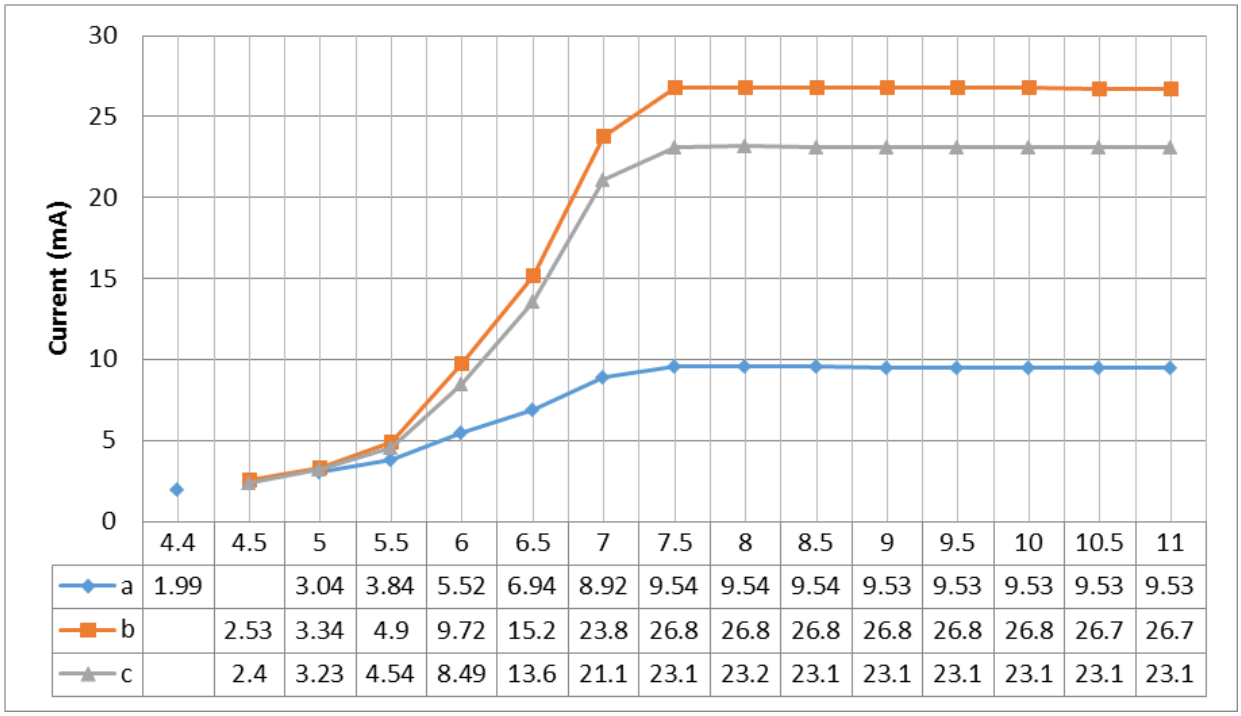


A	B	Y= (A+B)'
0	0	1
0	1	0
1	0	0
1	1	0

a) Current (mA). NOT powered. No inversions used. 1 LED on.

b) Current (mA). NOT powered. 3 inversions used. 4 LEDs on.

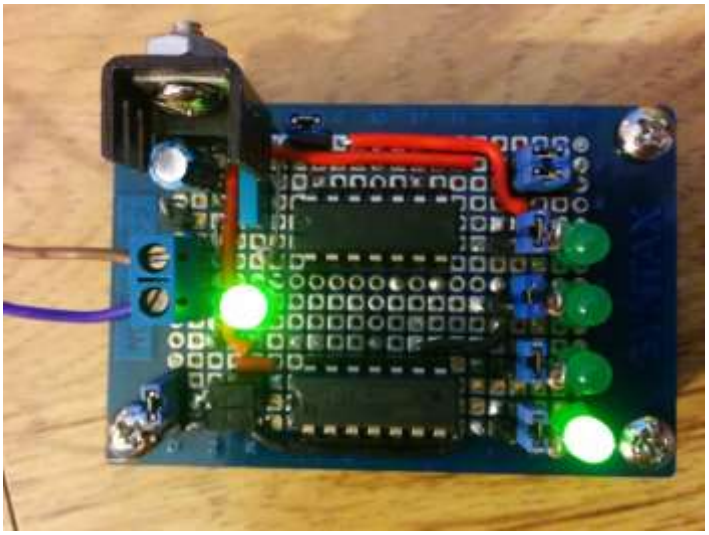
c) Current (mA). NOT powered. All inversions used. 3 LEDs on.



	4.4	4.5	5	5.5	6	6.5	7	7.5	8	8.5	9	9.5	10	10.5	11
a	1.99		3.04	3.84	5.52	6.94	8.92	9.54	9.54	9.54	9.53	9.53	9.53	9.53	9.53
b		2.53	3.34	4.9	9.72	15.2	23.8	26.8	26.8	26.8	26.8	26.8	26.8	26.7	26.7
c		2.4	3.23	4.54	8.49	13.6	21.1	23.1	23.2	23.1	23.1	23.1	23.1	23.1	23.1

Graph 4 – 7402 NOR gate current tendencies vs. Source Voltage Vs

7408 – Quad 2-input AND gate

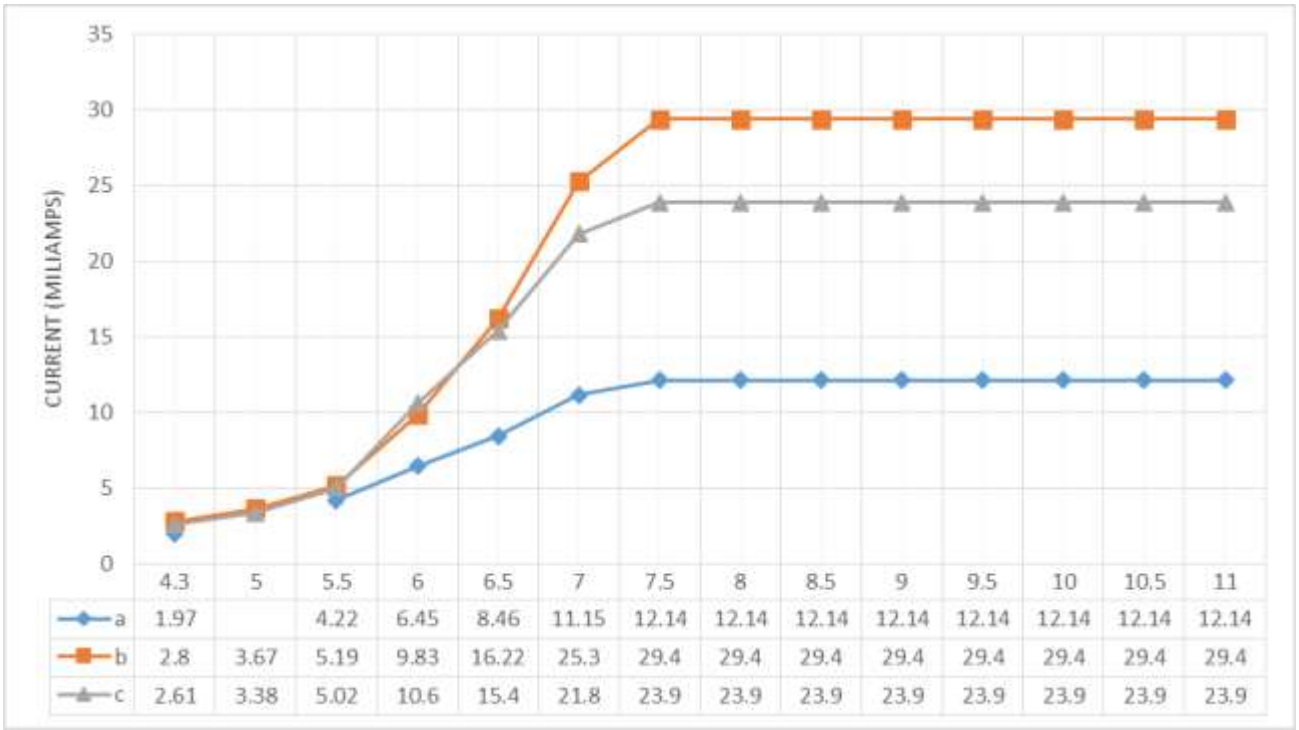


A	B	Y= AB
0	0	0
0	1	0
1	0	0
1	1	1

a) Current (mA). NOT powered. No inversions used. 1 LED on.

b) Current (mA). NOT powered. 3 inversions used. 4 LEDs on.

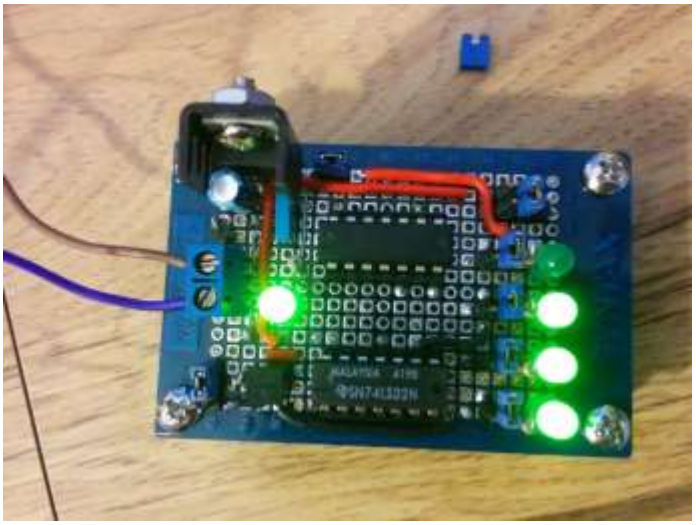
c) Current (mA). NOT powered. All inversions used. 3 LEDs on.



	4.3	5	5.5	6	6.5	7	7.5	8	8.5	9	9.5	10	10.5	11
a	1.97		4.22	6.45	8.46	11.15	12.14	12.14	12.14	12.14	12.14	12.14	12.14	12.14
b	2.8	3.67	5.19	9.83	16.22	25.3	29.4	29.4	29.4	29.4	29.4	29.4	29.4	29.4
c	2.61	3.38	5.02	10.6	15.4	21.8	23.9	23.9	23.9	23.9	23.9	23.9	23.9	23.9

Graph 5 – 7408 AND gate current tendencies vs. Source Voltage Vs

7432 – Quad 2-input OR gate

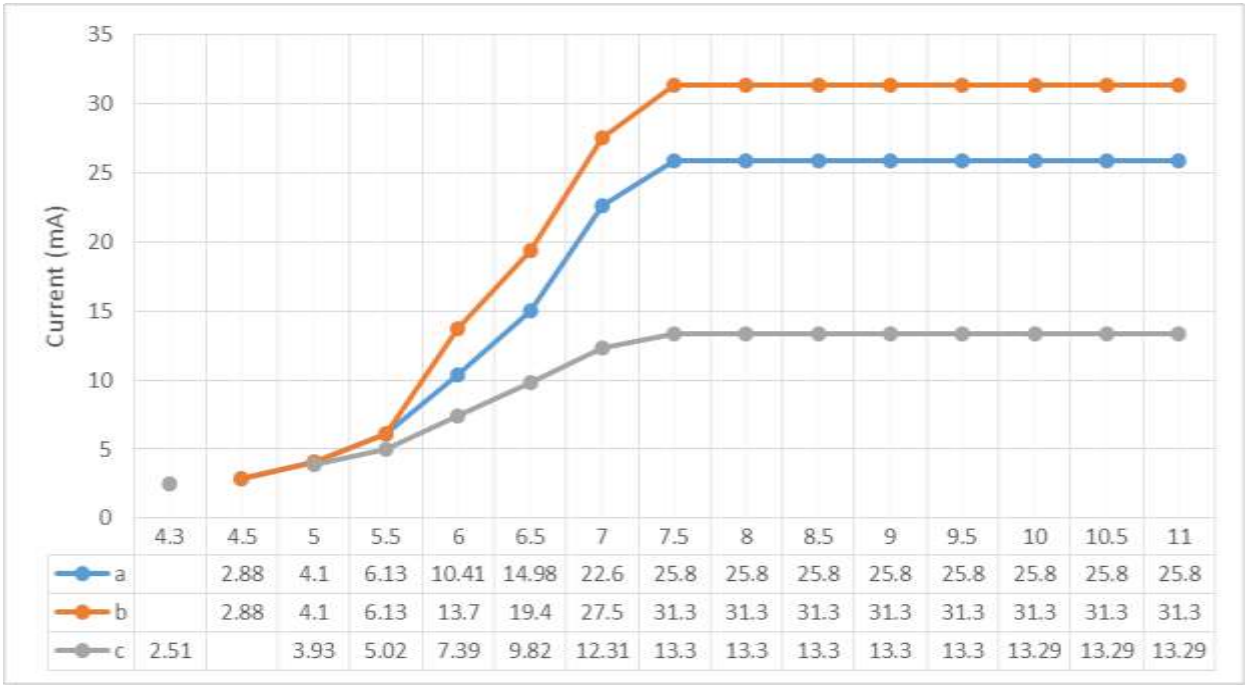


A	B	Y= A+B
0	0	0
0	1	1
1	0	1
1	1	1

a) Current (mA). NOT powered. No inversions used. 3 LED on.

b) Current (mA). NOT powered. 1 inversion used. 4 LEDs on.

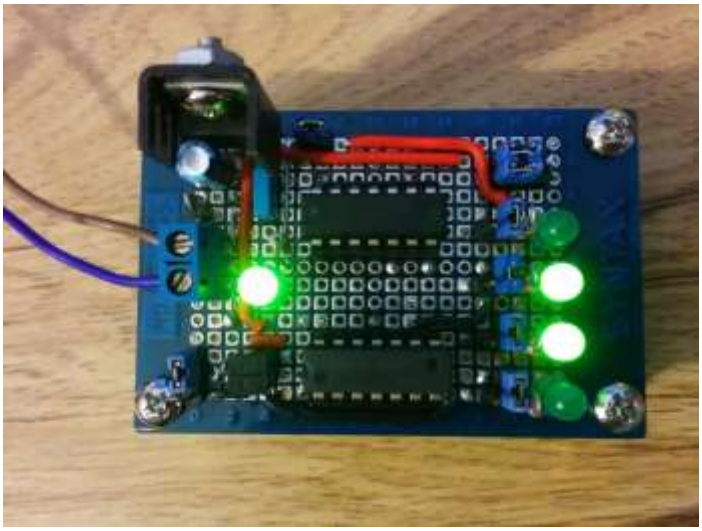
c) Current (mA). NOT powered. All inversions used. 1 LEDs on.



	4.3	4.5	5	5.5	6	6.5	7	7.5	8	8.5	9	9.5	10	10.5	11
a		2.88	4.1	6.13	10.41	14.98	22.6	25.8	25.8	25.8	25.8	25.8	25.8	25.8	25.8
b		2.88	4.1	6.13	13.7	19.4	27.5	31.3	31.3	31.3	31.3	31.3	31.3	31.3	31.3
c	2.51		3.93	5.02	7.39	9.82	12.31	13.3	13.3	13.3	13.3	13.3	13.29	13.29	13.29

Graph 6 – 7432 OR gate current tendencies vs. Source Voltage Vs

7486 – Quad 2-input XOR gate

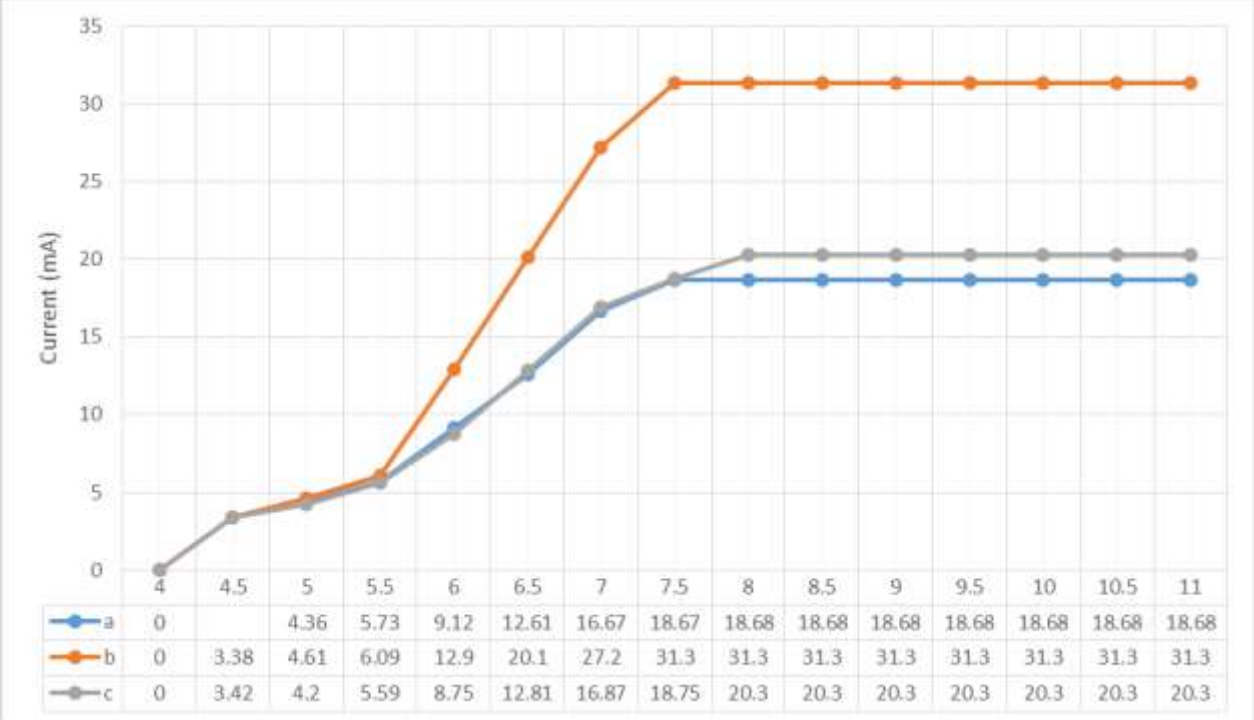


A	B	Y= AB'+A'B
0	0	0
0	1	1
1	0	1
1	1	0

a) Current (mA). NOT powered. No inversions used. 2 LED on.

b) Current (mA). NOT powered. 2 inversions used. 4 LEDs on.

c) Current (mA). NOT powered. All inversions used. 2 LEDs on.



	4	4.5	5	5.5	6	6.5	7	7.5	8	8.5	9	9.5	10	10.5	11
a	0		4.36	5.73	9.12	12.61	16.67	18.67	18.68	18.68	18.68	18.68	18.68	18.68	18.68
b	0	3.38	4.61	6.09	12.9	20.1	27.2	31.3	31.3	31.3	31.3	31.3	31.3	31.3	31.3
c	0	3.42	4.2	5.59	8.75	12.81	16.87	18.75	20.3	20.3	20.3	20.3	20.3	20.3	20.3

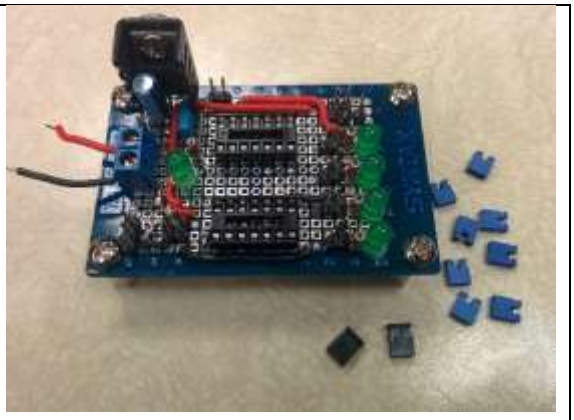
Graph 7 – 7486 XOR gate current tendencies vs. Source Voltage Vs

Datasheet

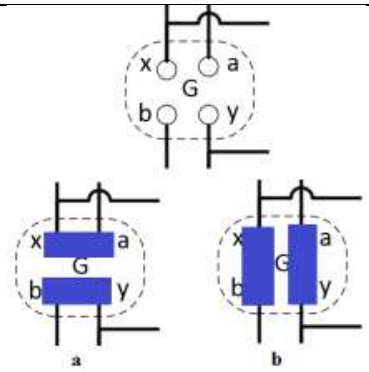
B.T.U.

Boolean Testing Unit

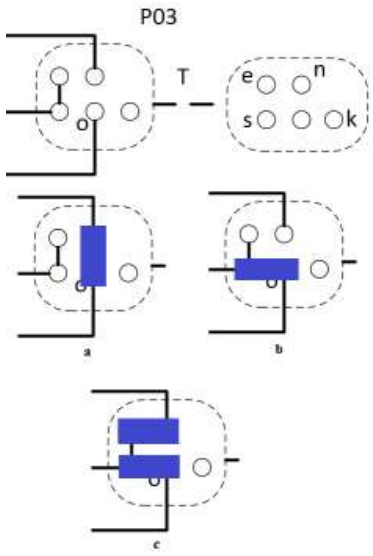
Testing prototype with built in DC power supply for exchangeable quad 2-input logic gates integrated circuits and truth table display



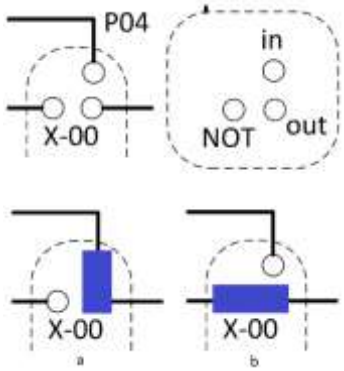
(tested)	@20°C	Minimum	Nominal	Maximum	Units
Voltage Regulator Module	Supply Voltage	4.5	9	12	V
	Output	2.5	5	5.03	V
	Supply Current (no load)	0.11	16.81	16.86	mA
Testing Module	NOR powered.				
	7400 load current	1.54	22.5	28.1	mA
	7402 load current	1.99	9.53	26.7	mA
	7408 load current	1.97	12.14	29.4	mA
	7432 load current	2.51	25.8	31.3	mA
	7486 load current	3.38	18.68	31.3	mA



NOR gate – x-b and a-y
All other – x-a and b-y



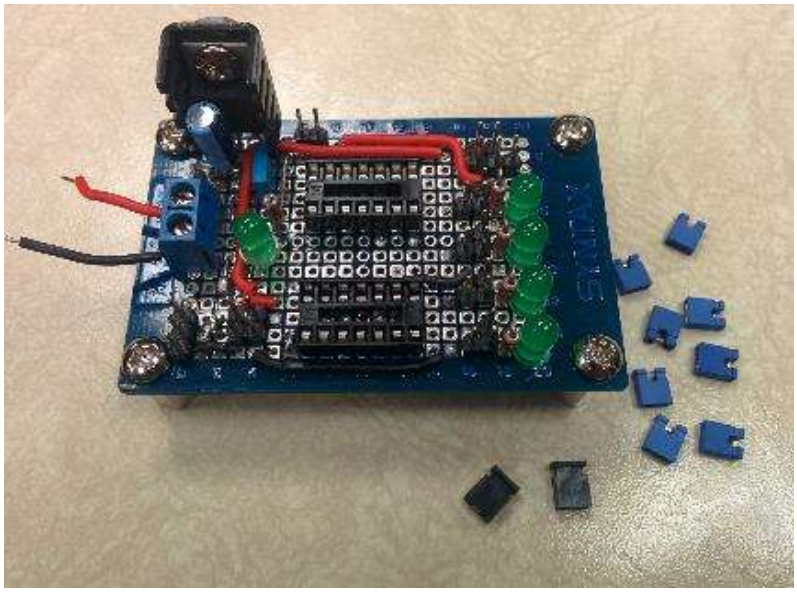
IC powered – o-n
NOT powered – o-s
Both powered – o-s and e-n



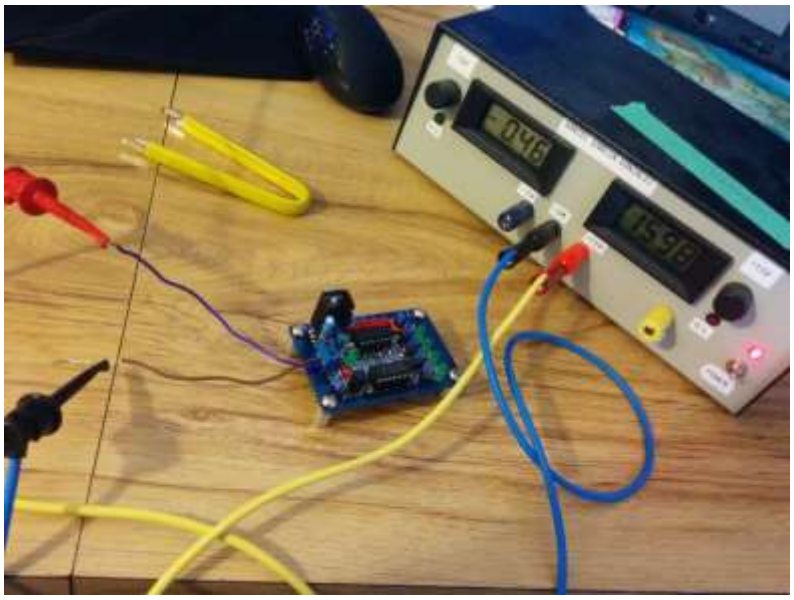
Direct output – in-out
Inverse output – NOT - out

Apex

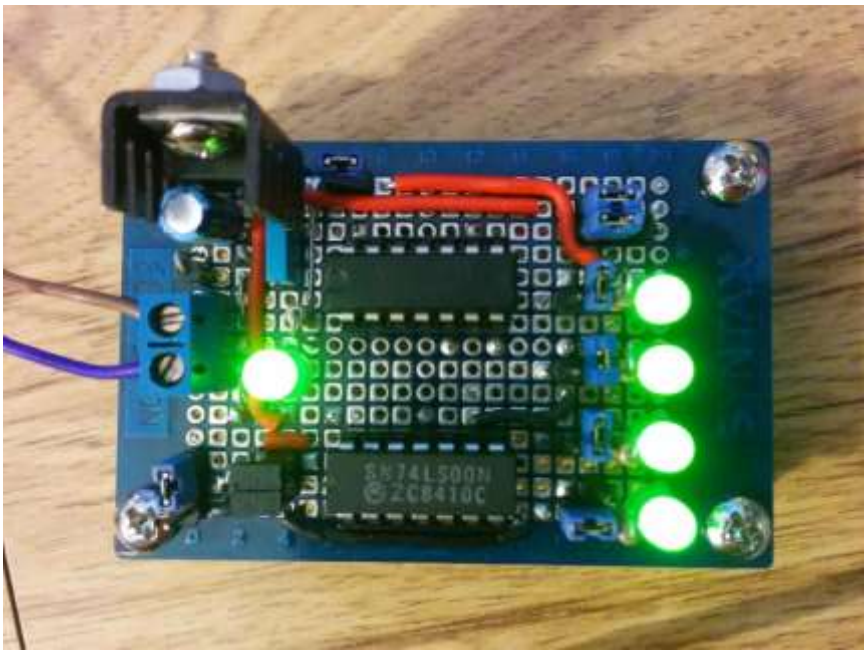
Additional testing and pictures



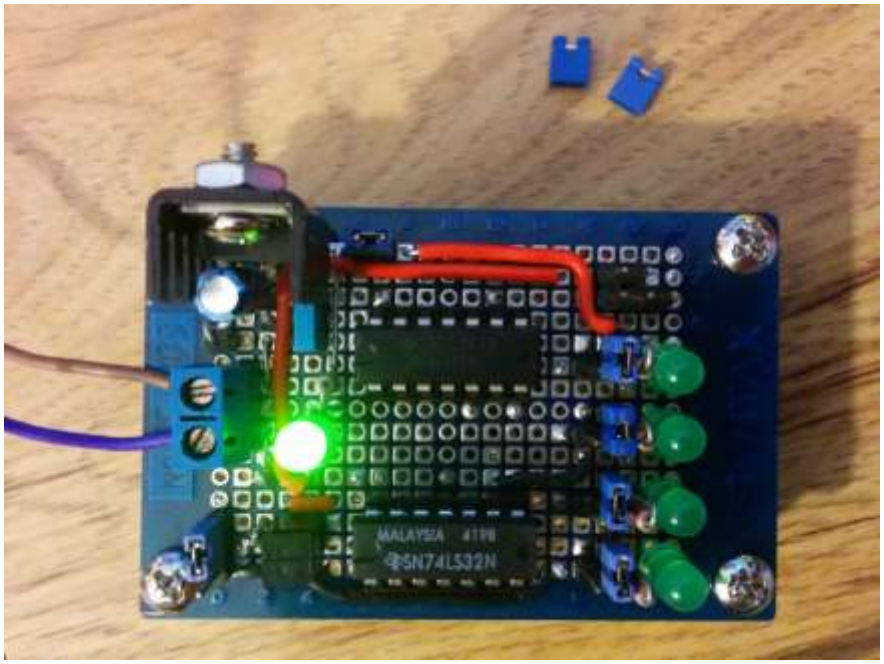
A1- Module with jumpers removed and no ICs connected. No power supplied



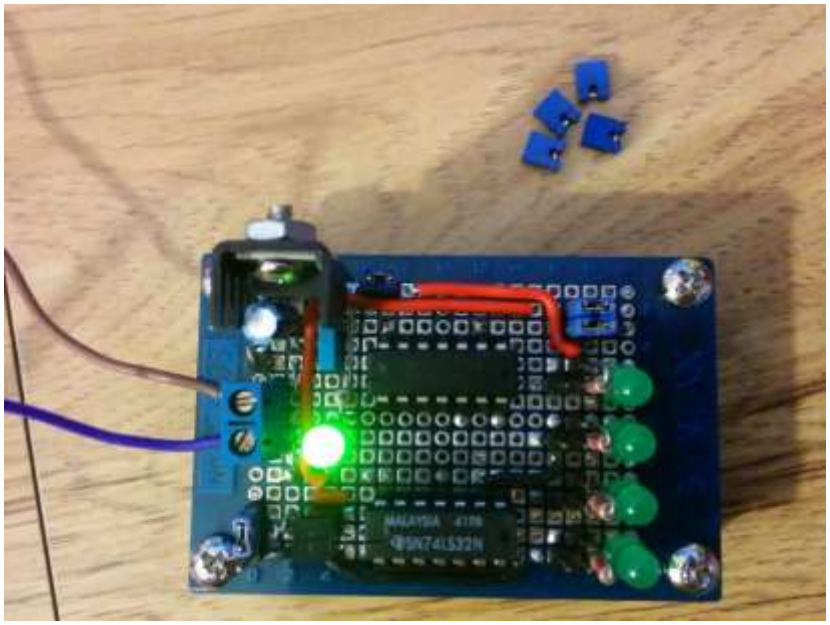
A2 – Reverse voltage testing. Up to 16V connected in inverse polarity with no signs of electric damage or overheating.



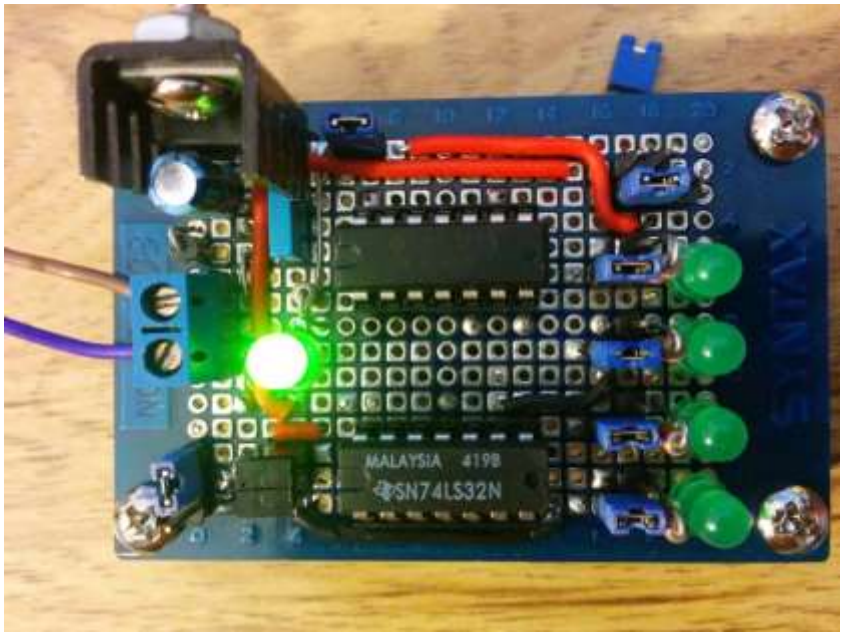
A3 – NAND gate with 1 inversion activated. 4 LEDs on



A4 – ON/OFF and Pin junction P02 jumper connected. No power is transmitted to the ICs because there's no jumper in P03 (IC selector)



A5 – On/OFF jumper, Junction P02 jumper, and IC selector P03 jumpers connected. Output LEDs' jumpers disconnected.



A6 – Only NOT IC socket powered. No usable output for proper testing