Driving a 5.0 Inch AVTFT LCD with C&T Video Controller

OBJECTIVE

This paper will focus on the LQ5AW116/ LQ5AW136, 5.0 inch AVTFT LCD and how it can be driven with a C&T 65545 video controller.

INTRODUCTION

SHARP AVTFT displays are generally meant to be driven with either a NTSC Composite Video or with discrete RGB Video signals. SHARP's AVTFTs have video compatible inputs that enable easy interfacing to a camcorder, a VCR, or the video output from a CCD camera. Most AVTFTs have two video input channels. One channel may be an NTSC Composite input and the other will be discrete RGB Video input. An example of this video input configuration is the LQ056A3CH01.

The LQ5AW116 is a dual video input channel AVTFT with discrete RGB inputs. It has a composite video input, but the display electronics merely use this input to strip off the sync information, disregarding the video content of the composite signal.

The LQ5AW116 was designed for discrete RGB video sources. It does not have an onboard video decoder. It requires an external video decoder IC like the SHARP IR3Y18A to make it compatible with NTSC video. However, if the user does not have a video source and wants to drive the LQ5AW116 with a flap panel video controller like a C&T, this paper will demonstrate a method of interfacing to the C&T 65545 video controller to drive either of the panel's RGB input channels.

LQ5AW116/136 OPERATION

The LQ5AW116 is an AVTFT (Audio Visual Thin Film Transistor) LCD. It can display one of two video input channels by making pin 7, VSW = HIGH (channel 1) or VSW = LOW (channel 2). The display can generate an LCD pixel clock internally or it can use an external clock depending on the setting of CLCK input. If the video signal input is NTSC decoded RGB, then CLCK = HIGH and an internal PLL will generate a pixel clock that is phase locked to the sync input. By doing this, pin 22 (CLK), pin 1 (H_{SYNC}) and pin 2 (V_{SYNC}) become outputs. If an RGB video signal is available and the user would like to control the LCD timing, set CLCK = LOW, making CLK, H_{SYNC}, and V_{SYNC} inputs.

Pin 8 (SAM) determines the external clock sampling mode. In Independent Data Sampling mode (pin 8 = HIGH), external clock (18.2 MHz to 19.6 MHz) is three times faster than in Simultaneous mode (pin 8 = LOW) and video data is sampled sequentially (first red, then green, and then blue). In Simultaneous mode, all three video inputs are sampled at the same point in time with a slower clock (6.8 MHz to 7.6 MHz).

C&T 65545 DESCRIPTION

The C&T video Controller is a highly integrated monolithic IC that integrates a flat panel-CRT VGA controller, a RAMDAC and a clock synthesizer. It has a Local Bus (32-bit CPU Direct or VL), an ISA interface and a PCI interface. It's Address, Data and Control lines interface to the MPU or MCU. It also interfaces with external memory (either 512KB or 1MB of video memory). It can output analog RGB video to a CRT Display or digital RGB video data to a Flat Panel Display. The system block diagram is illustrated in Figure 1.

The C&T 65545 has several categories of registers that control various interfacing, compatibility and display functions such as timing control and clock synthesis control to drive a flat panel or a CRT display. The Extension Registers (called 'XRs') are addressed with a 7-bit Extension Register Index. They are grouped according to the following functions:

- Miscellaneous registers
- Mapping registers
- Software flag registers
- Clock registers
- Multimedia registers
- BitBLT (Bit Block Transfers) registers
- Backwards compatibility registers
- Alternate horizontal and vertical registers
- Flat Panel registers

The C&T data book for the 65545 has a listing of the Extension Register names.

The vertical/horizontal timing control, pixel clock and analog video signals for the LQ5AW116 AVTFT display can be generated in the C&T 65545 by correctly configuring the extension registers. Appendix A is a sample listing of the extension register settings.

CLOCK SYNTHESIS

The 65545 has two programmable phase lock loop clock synthesizers to generate pixel clock (VCLK) and memory clock (MCLK). See the C&T data book for clock synthesizer PLL block diagram. VCLK has a table of three frequencies from which to select a frequency. Two of the table frequency values are fixed at 25.175 MHz and 28.322 MHz. The third frequency (CLK2) is programmable. The desired output frequency is defined by an 18-bit value programmed in XR30 - XR32. The C&T 65545 data sheet outlines parameters the user must derive to generate a desired pixel clock frequency.

Two equations with several variables control the output frequency of the pixel clock synthesizer.

Equation 1:

$$f_{OUT} = \frac{(f_{REF} \times 4 \times M)}{(PSN \times N \times 2\ p)}$$

Equation 2 :

$$f_{VCO} = \frac{(f_{REF} \times 4 \times M)}{(PSN \times N)}$$

where:

$$4\ MHz \le f_{REF} \le 20\ MHz$$

PSN is a prescaling factor that can be either 1 or 4.

M and N represent integer counter values where:

$$3 \le M \le 127,\ 3 \le N \le 127$$

The 65546 Data Book stipulates two other programming restrictions :

$$\frac{150\ kHz \le f_{REF}}{(PSN \times N) \le 2\ MHz}$$

and:

$$48\ MHz < f_{VCO} \le 220\ MHz$$

The restrictions are related to trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation.

XR30 - XR32 register settings shown in Appendix A were chosen based on the following choice of Parameters:

- Let f_{REF} = 7.373 MHz,
- Let PSN = 4 (this is the reference input frequency divisor), M = 92, N = 7: M/N = 13.14

Substituting into Equation 2:

$$f_{VCO} = \frac{(7.73\ MHz \times 4 \times 92)}{(4 \times 7)} = 96.9\ MHz$$

Substituting into Equation 1:

$$f_{OUT} = \frac{(7.73\ MHz \times 4 \times 92)}{(4 \times 7 \times 16)} = 6.056\ MHz$$

XR30 = 0000 1000 → 08h. Referring to page 121 of the 65545 data book:

- Bit D0 of XR30 is chosen to be '0' to enable divide by 4 for PSN (prescalar),
- Bits D3 - D1 are set to 100 to select Post Divisor = 16.

XR31 = 0101 1001 → 5Ah. Referring to page 168 of data book:

- M´ = (M – 2) = (92 – 2) = 90
- 90 = 5Ah.

XR32 = 0000 0101 → 05h. Referring to page 168:

- N´ = (N – 2) = (7 – 2) = 5
- 5 = 05h.

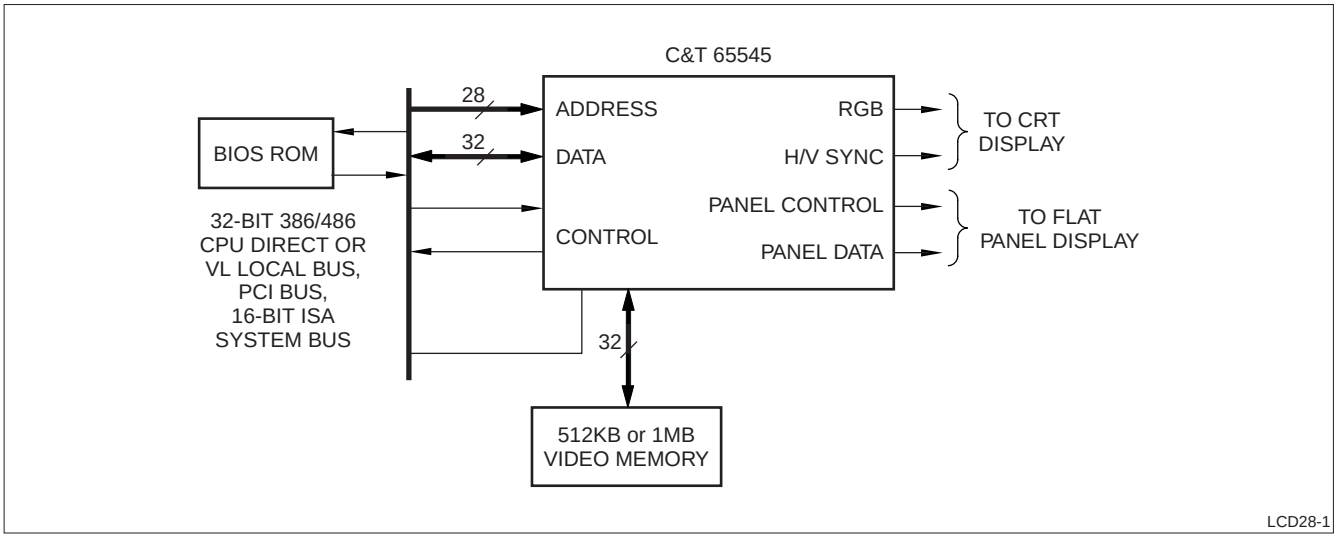

Figure 1. System Block Diagram

H_{SYNC} AND V_{SYNC} GENERATION

In the VGA and EGA modes of H_{SYNC} and V_{SYNC} timing is determined by the CRT Control Registers. For 320 column mode of operation the alternate XR registers are used. XR19, XR1A, XR1B are used to set up the H_{SYNC} period and pulse width. XR64, XR66, XR67 are used to configure V_{SYNC} timing.

VIDEO SIGNAL SELECTION

XR06 bit 1 = 0 enables the video DAC outputs. XR51 bit 2 = 1 enables the Flat Panel. If you select CRT mode by making bit 2 = 0, the SHFCLK output is disabled. So, operating in the Flat Panel mode with CRT video outputs enabled sets up the correct operating conditions to drive the LQ5AW116 with external timing/control and video.

VIDEO BIOS ROM INTERFACE

All of the register settings for the C&T 65545 are part of the Video BIOS that usually resides in an external ROM chip. An 8-bit BIOS is implemented with one external ROM or can be part of the system BIOS that may reside in a Flash memory chip. When the system boots up, the C&T registers are configured according to Video BIOS settings. C&T supplies a standard BIOS that supports flat panel and CRT displays. Modifications to the BIOS can be made by using the BIOS Modification Program (BMP) to program the extended functions or make any register changes required by a specific application.

VIDEO CONTROLLER AND LCD INTERFACING

In most LCD panel applications the video interface to the LCD is digital, especially if the LCD is a color TFT. However, in this case the video controller's digital video outputs on P0 - P7 were not used. Instead, the CRT analog video outputs were chosen to drive the LCD's channel 2 video inputs. Pull down resistors were added to the video output of the controller to minimize the peak signal amplitude going to the LCD. Maximum signal amplitude for Video RGB inputs needs to be limited to 0.7 V_{PP} .

Figure 2 shows the wiring diagram connecting the video controller to the LCD.

SUMMARY

SHARP's LQ5AW116 and the LQ056A3CH01 have discrete analog RGB video inputs. Both displays can generate their own clock, provided a composite video signal is available to provide Sync information to the LCDs. Both displays can also clock in analog video data using externally generated V_{SYNC}, H_{SYNC}, and pixel clock. The C&T 65545 video controller configured in the Flat Panel Mode with CRT outputs enabled can drive either of the LQ5AW116's analog RGB video channels. Other methods of generating timing, such as the use of an FPGA circuit will work also, provided the video data is sampled with the correct phase of the clock.

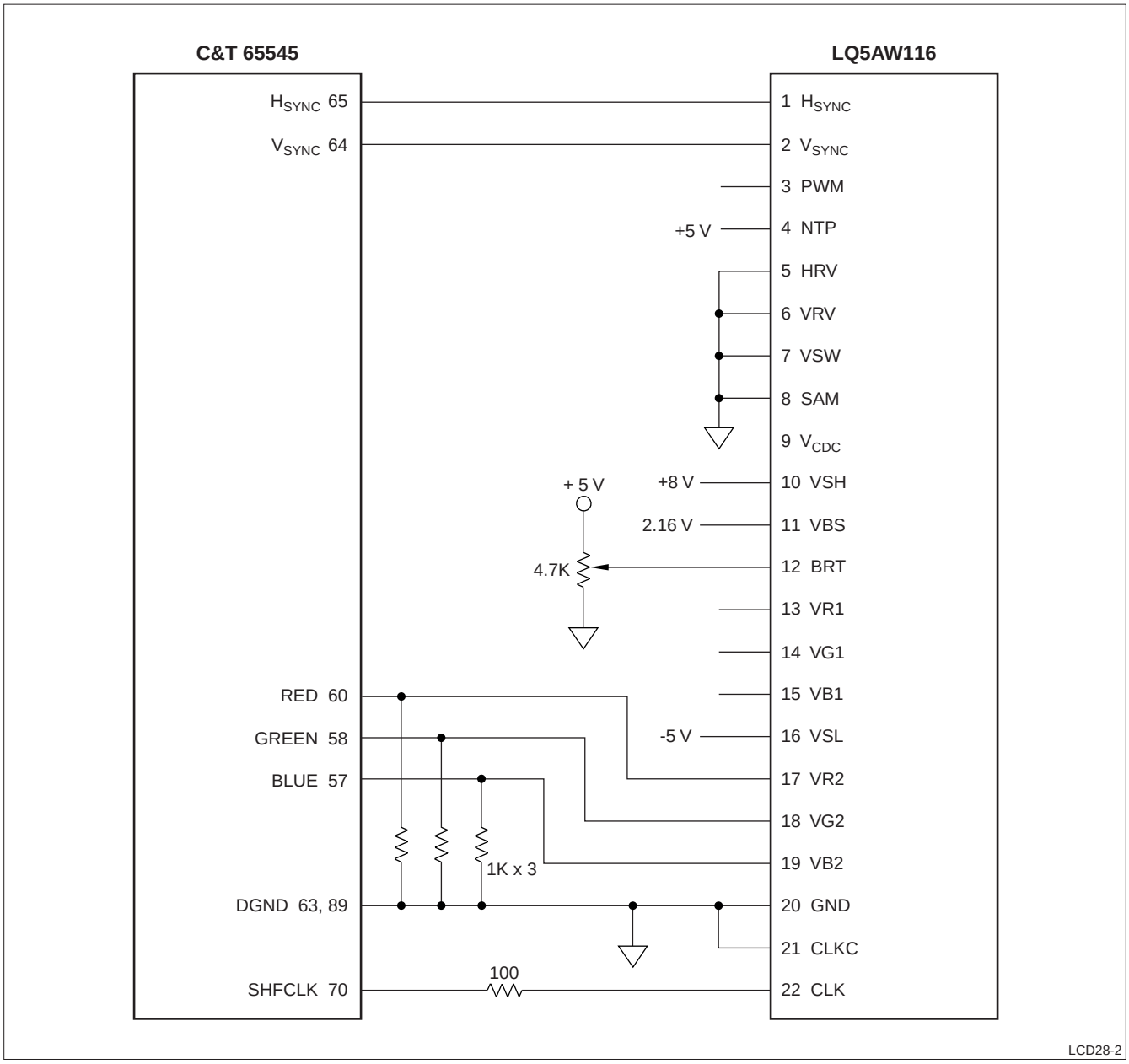

Figure 2. System Wiring Diagram

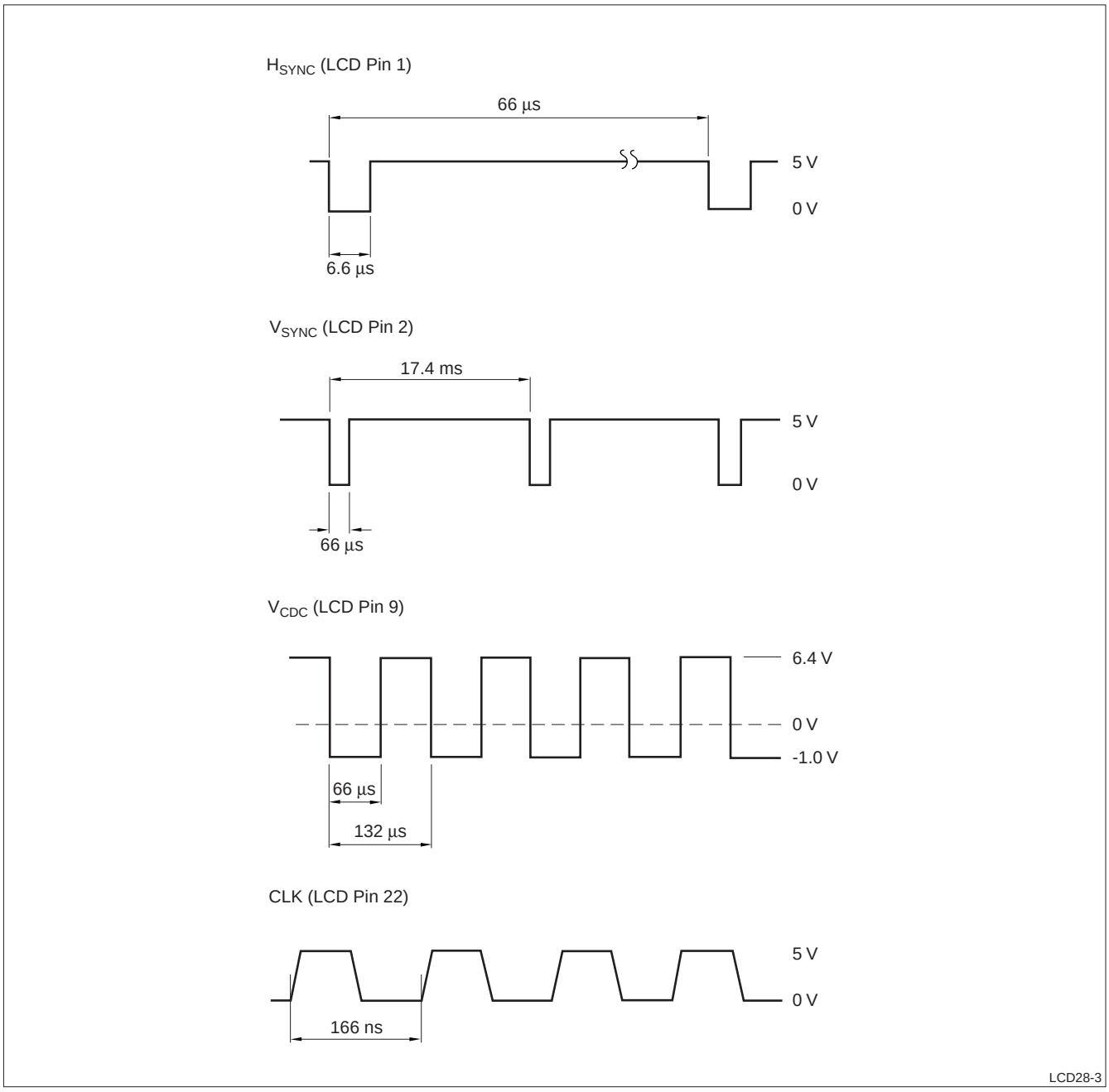

Figure 3. LQ5AW116 Timing Diagrams

APPENDIX A

Table 1. Register Settings for C&T 65545 Configured to drive SHARP LQ5AW116 AVTFT

XR00	DA	XR01	FD	XR02	81	XR03	02	XR04	21	XR05	00	XR06	40	XR07	74
XR08	04	XR09	00	XR0A	00	XR0B	15	XR0C	00	XR0D	00	XR0E	80	XR0F	00
XR10	00	XR11	00	XR12	00	XR13	00	XR14	00	XR15	00	XR16	00	XR17	00
XR18	00	XR19	28	XR1A	0B	XR1B	2F	XR1C	27	XR1D	00	XR1E	50	XR1F	00
XR20	00	XR21	00	XR22	00	XR23	00	XR24	00	XR25	00	XR26	00	XR27	00
XR28	10	XR29	00	XR2A	00	XR2B	00	XR2C	12	XR2D	2A	XR2E	2A	XR2F	04
XR30	08	XR31	5A	XR32	05	XR33	00	XR34	00	XR35	00	XR36	00	XR37	00
XR38	00	XR39	00	XR3A	00	XR3B	00	XR3C	00	XR3D	00	XR3E	00	XR3F	00
XR40	01	XR41	00	XR42	00	XR43	00	XR44	00	XR45	00	XR46	00	XR47	00
XR48	00	XR49	00	XR4A	00	XR4B	00	XR4C	00	XR4D	00	XR4E	00	XR4F	07
XR50	00	XR51	04	XR52	01	XR53	0C	XR54	28	XR55	C0	XR56	00	XR57	00
XR58	00	XR59	00	XR5A	00	XR5B	11	XR5C	00	XR5D	00	XR5E	80	XR5F	00
XR60	83	XR61	00	XR62	00	XR63	00	XR64	05	XR65	01	XR66	F4	XR67	05
XR68	F0	XR69	00	XR6A	00	XR6B	00	XR6C	0B	XR6D	00	XR6E	56	XR6F	00
XR70	00	XR71	00	XR72	FE	XR73	00	XR74	00	XR75	00	XR76	00	XR77	00
XR78	00	XR79	00	XR7A	00	XR7B	00	XR7C	00	XR7D	00	XR7E	00	XR7F	00
SR00	03	SR01	01	SR02	0F	SR03	00	SR04	0E	SR05	00	SR06	00	SR07	00
GR00	00	GR01	00	GR02	00	GR03	00	GR04	00	GR05	00	GR06	05	GR07	0F
CR00	5F	CR01	4F	CR02	50	CR03	82	CR04	54	CR05	80	CR06	0B	CR07	3E
CR08	00	CR09	40	CR0A	00	CR0B	00	CR0C	00	CR0D	00	CR0E	00	CR0F	00
CR10	EA	CR11	0C	CR12	DF	CR13	50	CR14	00	CR15	E7	CR16	04	CR17	E3
CR18	FF	CR19	00	CR1A	00	CR1B	00	CR1C	00	CR1D	00	CR1E	00	CR1F	00
CR20	00	CR21	00	CR22	FF	CR23	00	CR24	80	CR25	00	CR26	00	CR27	00
CR28	00	CR29	00	CR2A	00	CR2B	00	CR2C	00	CR2D	00	CR2E	00	CR2F	00
CR30	00	CR31	00	CR32	00	CR33	00	CR34	00	CR35	00	CR36	00	CR37	00
CR38	00	CR39	00	CR3A	00	CR3B	00	CR3C	00	CR3D	00	CR3E	00	CR3F	00
CR40	5F	CR41	4F	CR42	50	CR43	82	CR44	54	CR45	80	CR46	0B	CR47	3E
CR48	00	CR49	40	CR4A	00	CR4B	00	CR4C	00	CR4D	00	CR4E	00	CR4F	00
CR50	EA	CR51	0C	CR52	DF	CR53	50	CR54	00	CR55	E7	CR56	04	CR57	E3
CR58	FF	CR59	00	CR5A	00	CR5B	00	CR5C	00	CR5D	00	CR5E	00	CR5F	00
CR60	00	CR61	00	CR62	FF	CR63	00	CR64	80	CR65	00	CR66	00	CR67	00
CR68	00	CR69	00	CR6A	00	CR6B	00	CR6C	00	CR6D	00	CR6E	00	CR6F	00
CR70	00	CR71	00	CR72	00	CR73	00	CR74	00	CR75	00	CR76	00	CR77	00
CR78	00	CR79	00	CR7A	00	CR7B	00	CR7C	00	CR7D	00	CR7E	00		
AR00	00	AR01	01	AR02	02	AR03	03	AR04	04	AR05	05	AR06	06	AR07	07
AR08	08	AR09	09	AR0A	0A	AR0B	0B	AR0C	0C	AR0D	0D	AR0E	0E	AR0F	0F
AR10	01	AR11	00	AR12	0F	AR13	00	AR14	00	AR15	00	AR16	00	AR17	00

Table 2. Register Settings for C&T 65545
Configured to drive SHARP LQ5AW116 AVTFT

PL00-FC, 00, 00	PL01-DC, 00, 00	PL02-BC, 00, 00	PL03-9C, 00, 00
PL04-7C, 00, 00	PL05-5C, 00, 00	PL06-FC, 80, 00	PL07-DC ,70, 00
PL08-BC ,60 ,00	PL09-9C, 50, 00	PL0A-7C, 40, 00	PL0B-5C, 30, 00
PL0C-FC, F8, 00	PL0D-DC, D8, 00	PL0E-BC, B8, 00	PL0F-9C, 98, 00
PL10-7C, 78, 00	PL11-5C, 58, 00	PL12-80, F8, 00	PL13-70, D8, 00
PL14-60, B8, 00	PL15-50, 98, 00	PL16-40, 78, 00	PL17-30, 58, 00
PL18-00, F8, 00	PL19-00, D8, 00	PL1A-00, B8, 00	PL1B-00, 98, 00
PL1C-00, 78, 00	PL1D-00, 58, 00	PL1E-00, F8, 80	PL1F-00, D8, 70
PL20-00, B8, 60	PL21-00, 98, 50	PL22-00, 78, 40	PL23-00, 58, 30
PL24-00, F8, FC	PL25-00, D8, DC	PL26-00, B8, BC	PL27-00, 98, 9C
PL28-00, 78, 7C	PL29-00, 58, 5C	PL2A-00, 80, FC	PL2B-00, 70, DC
PL2C-00, 60, BC	PL2D-00, 50, 9C	PL2E-00, 40, 7C	PL2F-00, 30, 5C
PL30-00, 00, FC	PL31-00, 00, DC	PL32-00, 00, BC	PL33-00, 00, 9C
PL34-00, 00, 7C	PL35-00, 00, 5C	PL36-80, 00, FC	PL37-70, 00, DC
PL38-60, 00, BC	PL39-50, 00, 9C	PL3A-40, 00, 7C	PL3B-30, 00, 5C
PL3C-FC, 00, FC	PL3D-DC, 00, DC	PL3E-BC, 00, BC	PL3F-9C, 00, 9C
PL40-7C, 00, 7C	PL41-5C, 00, 5C	PL42-FC, 00, 80	PL43-DC, 00, 70
PL44-BC, 00, 60	PL45-9C, 00, 50	PL46-7C, 00, 40	PL47-5C, 00, 30
PL48-FC, F8, FC	PL49-EC, E8, EC	PL4A-CC, C8, CC	PL4B-A8, A8, A8
PL4C-88, 88, 88	PL4D-64, 60, 64	PL4E-B8, B8, B8	PL4F-98, 98, 98
PL50-74, 70, 74	PL51-54, 50, 54	PL52-30, 30, 30	PL53-20, 20, 20
PL54-DC, D8, DC	PL55-44, 40, 44	PL56-10, 10, 10	PL57-00, 00, 00
PL58-00, 00, 00	PL59-00, 00, 00	PL5A-00, 00, 00	PL5B-00, 00, 00
PL5C-00, 00, 00	PL5D-00, 00, 00	PL5E-00, 00, 00	PL5F-00, 00, 00
MSR	2B		

REFERENCES:

Chips and Technologies Inc. 65540/545 Data Sheet
Revision 1.2 (Oct. 95).

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